AN-002
APPLICATION NOTE

APx585 DSIO Setup

for optimal operation with the LnK SLIMbus Audio Bridge

APx585 shown with Digital Serial I/O and HDMI options

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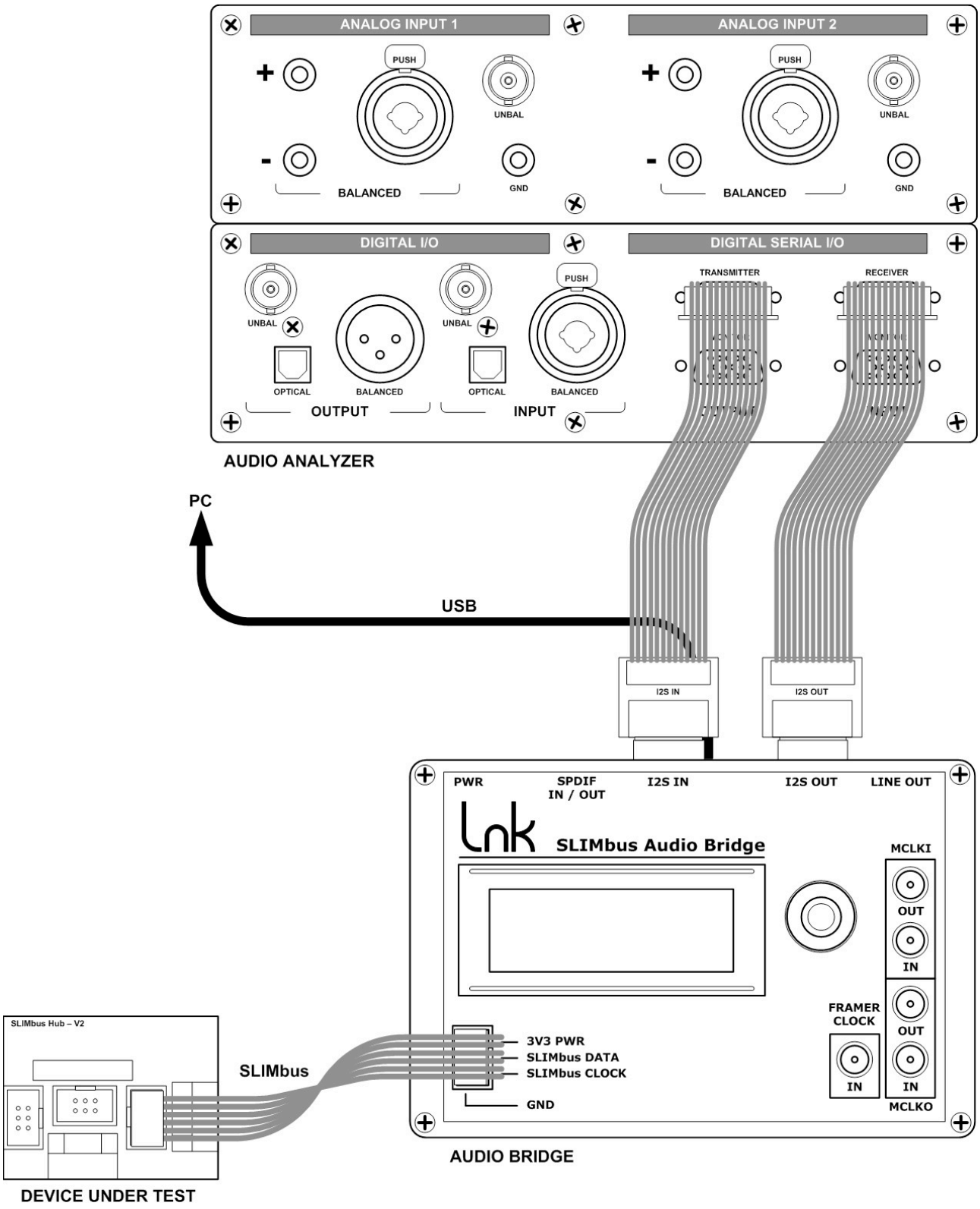
1. Purpose of the document

This document will guide the user through the setup of the DSIO transmitter and receiver of the APx585 audio analyzer from Audio Precision. The procedure will also apply to the APx525 but only 2 channels at a time can be analyzed. Both clock and data options will be detailed.

A basic knowledge of the operation of the SLIMbus Audio Bridge and the APx585 is required to follow the various explanations given in this document. Refer to the SLIMbus Audio Bridge HW and SW user manuals, the APx500 user manual and the APx DSIO datasheet for more information about these equipments.

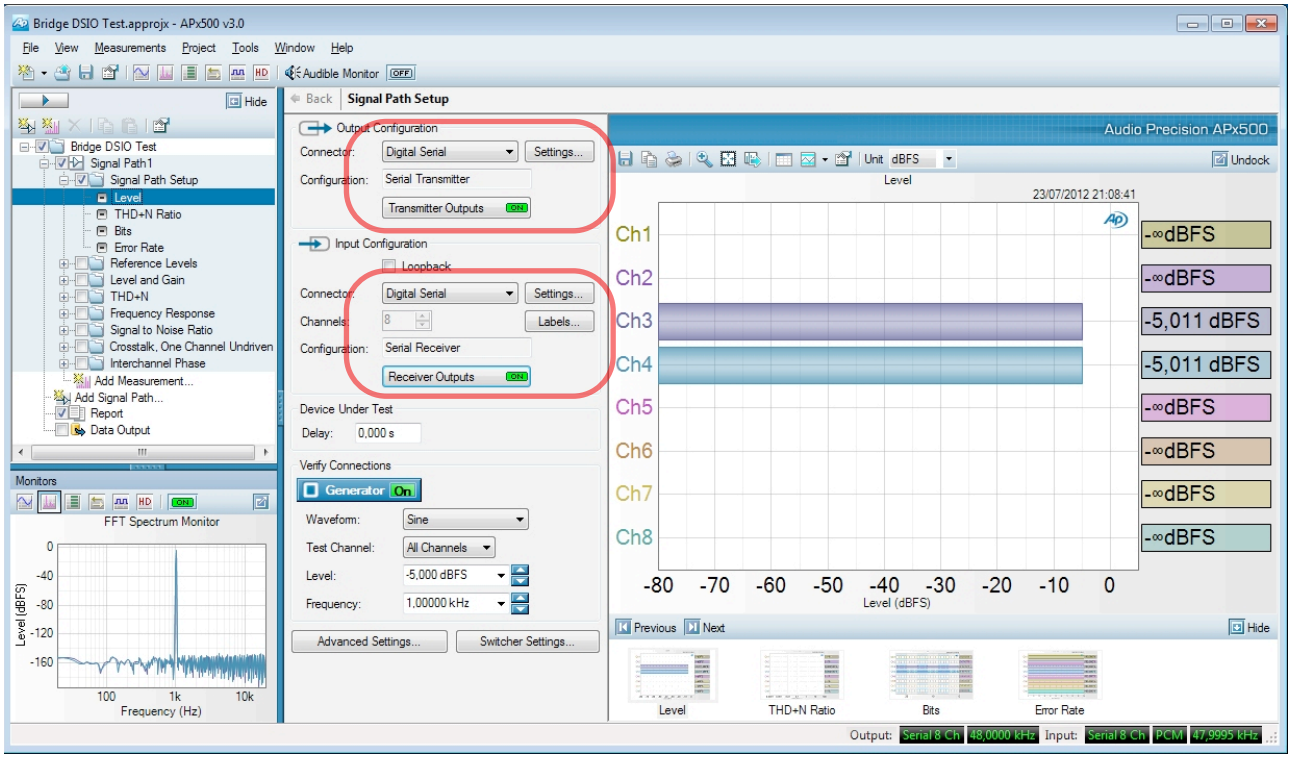
2. Typical Setup

The LnK SLIMbus Bridge is used to inject or receive digital audio on SLIMbus. It allows the APx585 to directly feed a signal to a SLIMbus audio device and / or to receive and analyze an audio signal coming from a SLIMbus audio device.



The DSIO transmitter is connected to the bridge I2S input.
The DSIO receiver is connected to the bridge I2S output.

In the main window of the APx500 software, the user can select the APx signal path. In the SIgnal Path Setup pane, select “Digital Serial” for the desired connector. For the targeted measurement, it could be the Output connector, the Input connector or both.

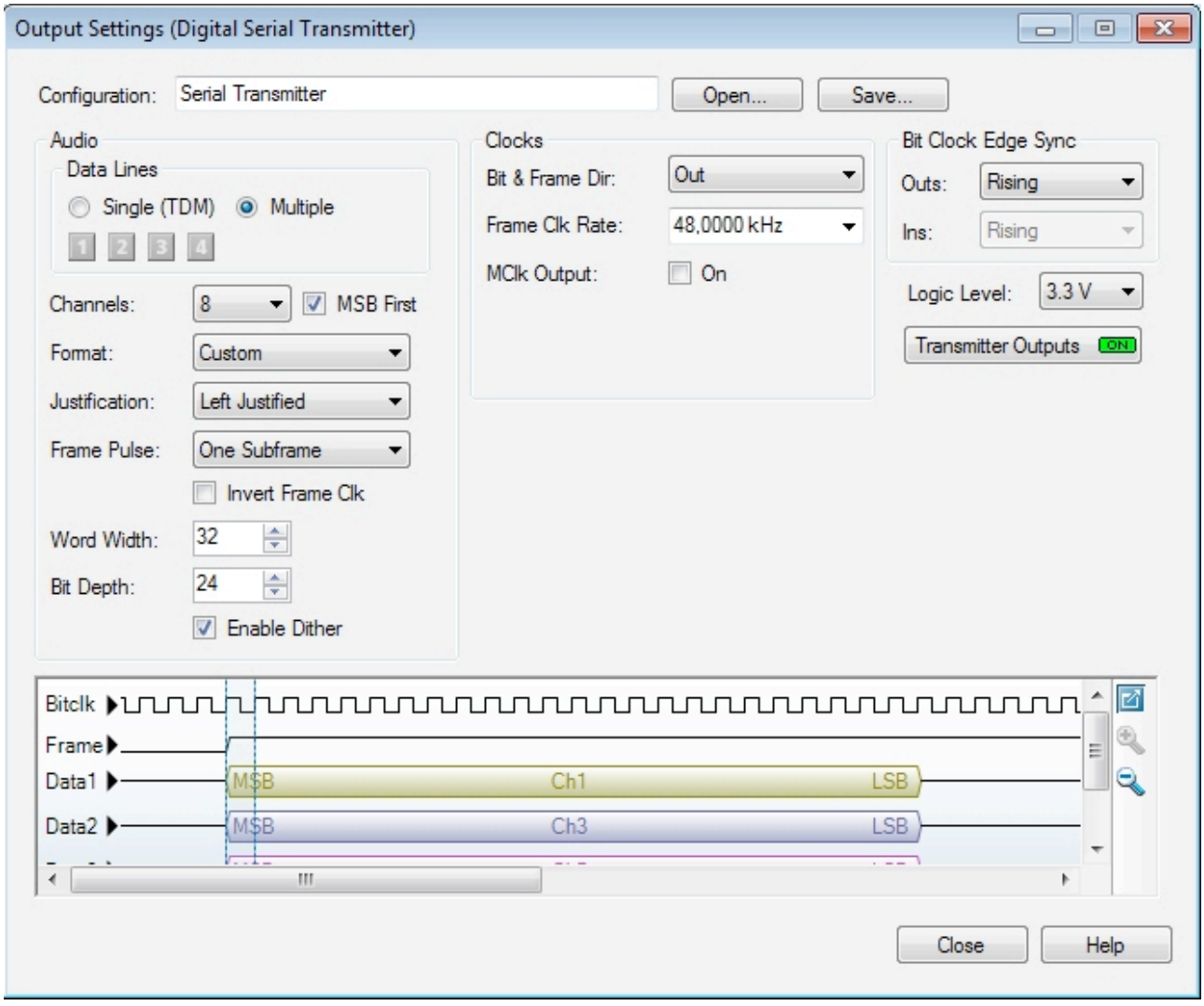


The LnK SLIMbus Audio Bridge uses the “Left Justified” format on 4 data lines sharing the same bit clock and word clock.

3. DSIO Transmitter Setup

The I2S input of the LnK SLIMbus Audio Bridge is **slave**. This means that it must receive the bit clock and the word clock from the APx585. Therefore, the "**Bit and Frame Dir**" shall be set to "**Out**".

The bridge takes its 8 data streams from 4 data lines. Select "**Multiple**" data lines instead of "**Single (TDM)**". There are "**8**" channels and the data are transmitted MSb first.
The justification is "**Left Justified**".
The word clock must have a duty cycle of 50%. Set "**Framer Pulse**" to "**One Subframe**".
The frame size is always 64 bits (32 bits for the channel A and 32 bits for channel B). Set the "**Word Width**" to "**32**". The maximum "**Bit Depth**" of the data received by the bridge is "**24**".
The "**Bit Clock Edge**" is set by default to "**Rising**".
The "**Logic Level**" (signaling voltage) must be set to "**3.3V**".

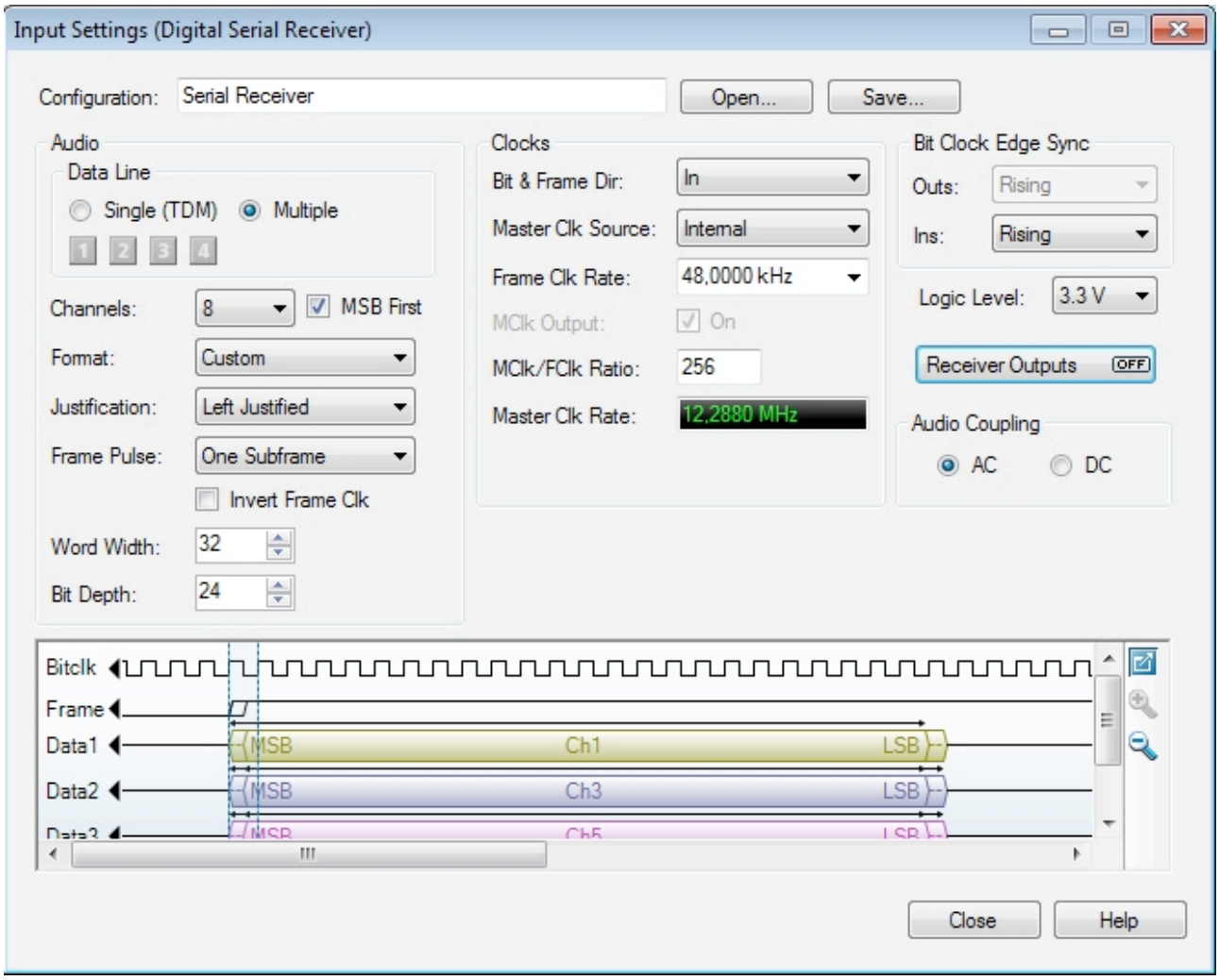


Make sure that the DSIO transmitter outputs are "**ON**".

4. DSIO Receiver Setup

The I2S output of the LnK SLIMbus Audio Bridge is **master**. This means that it will transmit the bit clock and the word clock to the APx585. Therefore, the "**Bit and Frame Dir**" shall be set to "**In**".

The bridge transmits its 8 data streams over 4 data lines. Select "**Multiple**" data lines instead of "**Single (TDM)**". There are "**8**" channels and the data are transmitted MSb first.
The justification is "**Left Justified**". The word clock must have a duty cycle of 50%. Set "**Framer Pulse**" to "**One Subframe**".
The frame size is always 64 bits (32 bits for the channel A and 32 bits for channel B). Set the "**Word Width**" to "**32**". The maximum "**Bit Depth**" of the data received by the bridge is "**24**".
The "**Bit Clock Edge**" is set by default to "**Rising**".
The "**Logic Level**" (signaling voltage) must be set to "**3.3V**".

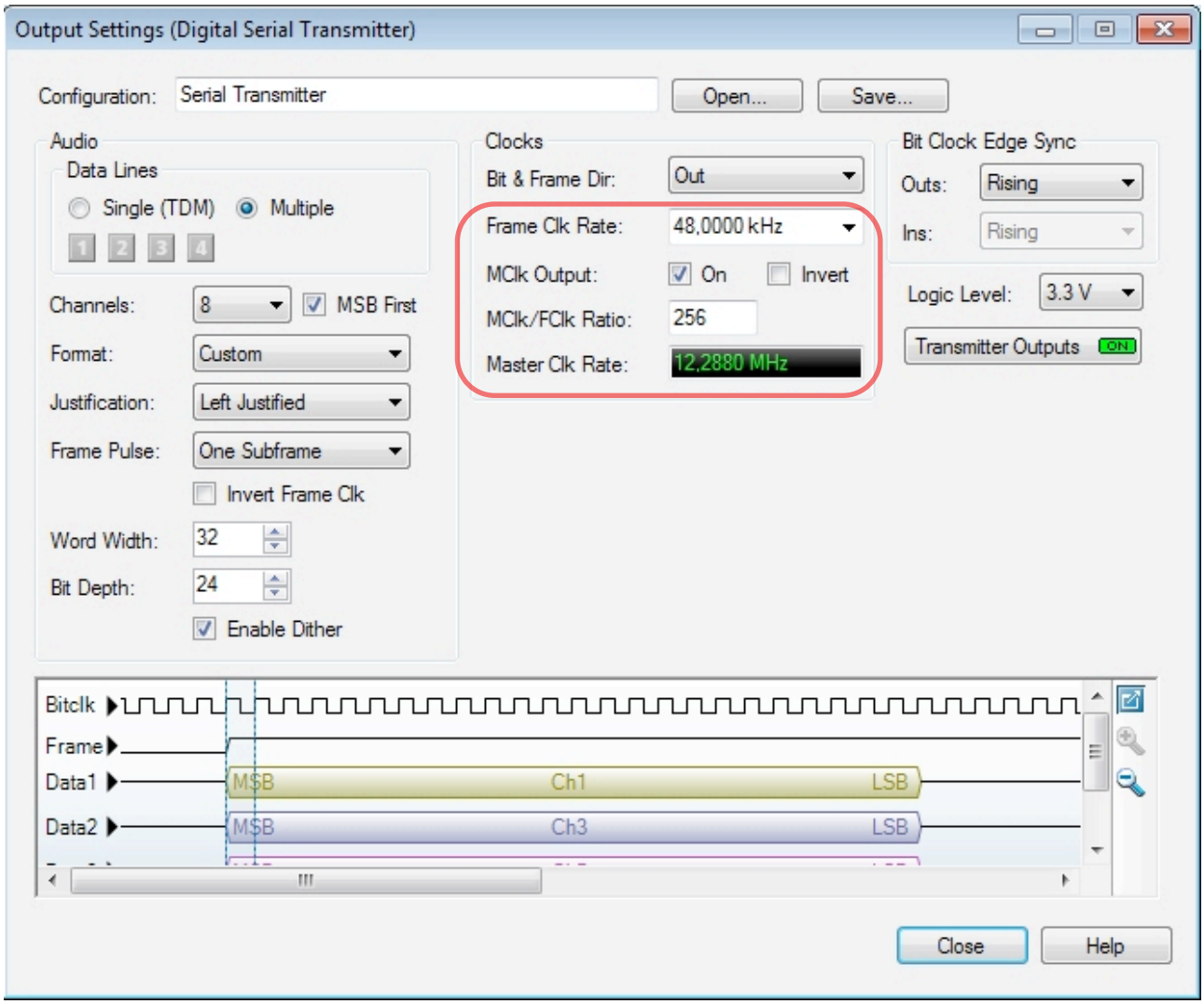


The DSIO transmitter outputs should normally be "**OFF**".

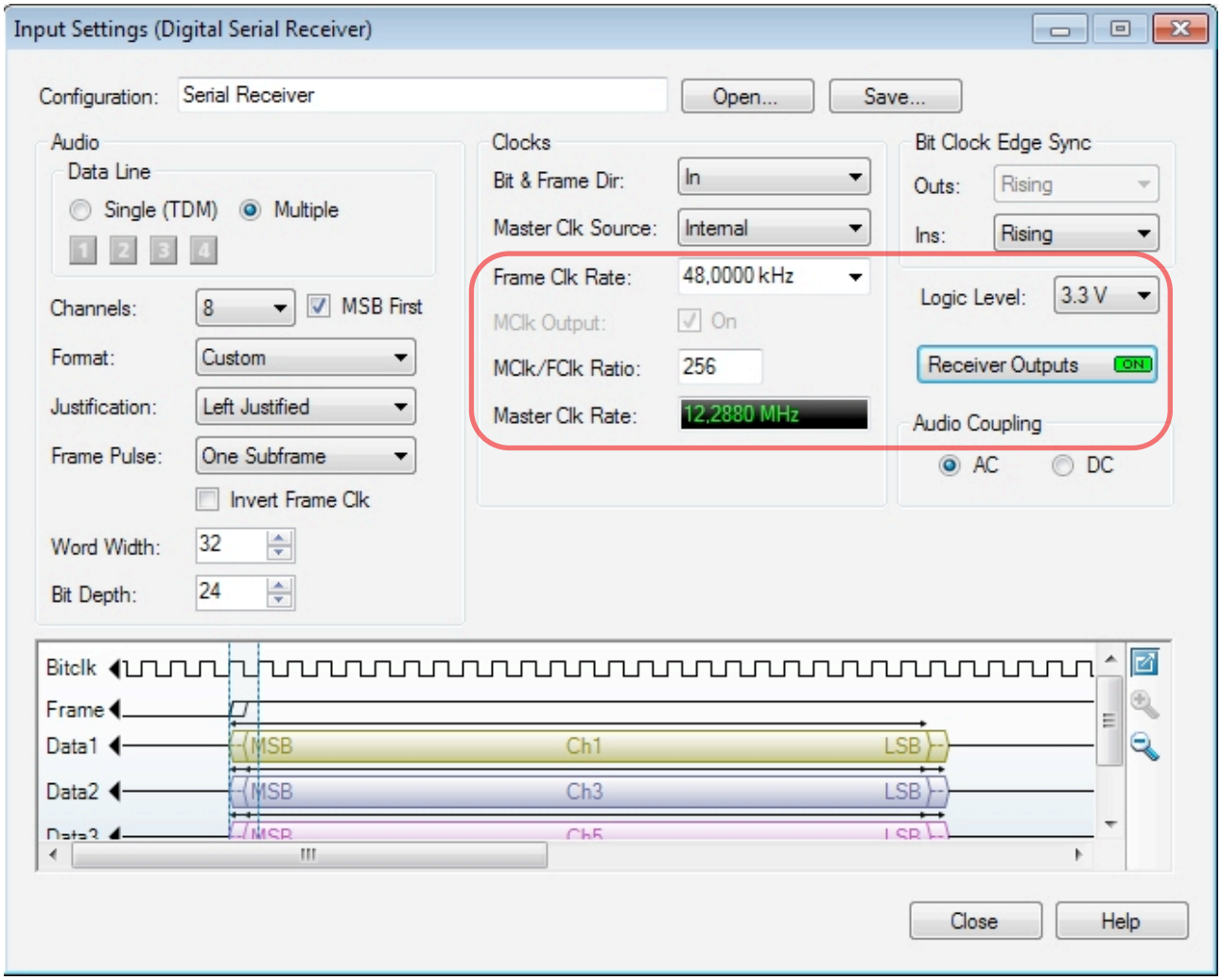
5. DSIO Master clock setup

The LnK SLIMbus Audio Bridge has the ability to receive its audio master clock from the DSIO transmitter and receiver interfaces. Refer to the application note **"Audio Bridge Clock Management"** for more information about using external clocks.

To enable the DSIO Transmitter output clock, click on the check box "**ON**" besides the "**MClk Output**". The "**MClk/FClk Ratio**" must be equal to "**256**" for all sampling rates lower or equal to 96 kHz. It must be equal to "**128**" for the sampling rates greater than 96 kHz. The effective Master Clock frequency can be read in the "**Master Clock Rate**" field.



To enable the DSIO receiver output clock, specify the right expected sampling rate ("**Frame Clk Rate**") and the "**MClk/FClk Ratio**" which must be equal to "**256**" for all sampling rates lower or equal to 96 kHz and must be equal to "**128**" for the sampling rates greater than 96 kHz.
Make sure that the "**Receiver Outputs**" are "**ON**"

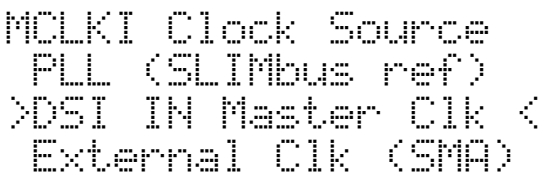

Input Settings (Digital Serial Receiver)
Configuration:
Serial Receiver
Open...
Save...
Audio
Data Line
Single (TDM)
Multiple
1
2
3
4
Channels:
8
MSB First
Format:
Custom
Justification:
Left Justified
Frame Pulse:
One Subframe
Invert Frame Clk
Word Width:
32
Bit Depth:
24
Clocks
Bit & Frame Dir:
In
Master Clk Source:
Internal
Frame Clk Rate:
48,0000 kHz
MClk Output:
On
MClk/FClk Ratio:
256
Master Clk Rate:
12,2880 MHz
Bit Clock Edge Sync
Outs:
Rising
Ins:
Rising
Logic Level:
3.3 V
Receiver Outputs
ON
Audio Coupling
AC
DC
BitClk
Frame
Data1
Data2
MSB
Ch1
Ch3
LSB
Close
Help

6. Bridge Clock Input Selection

The SLIMbus Audio Bridge clock source can be set by using the bridge configuration menu itself or via the PC control software.

Bridge configuration menu:
- Press the rotary knob.
- Rotate the knob to reach "**Select MCLKI src**" or "**Select MCLKO src**".

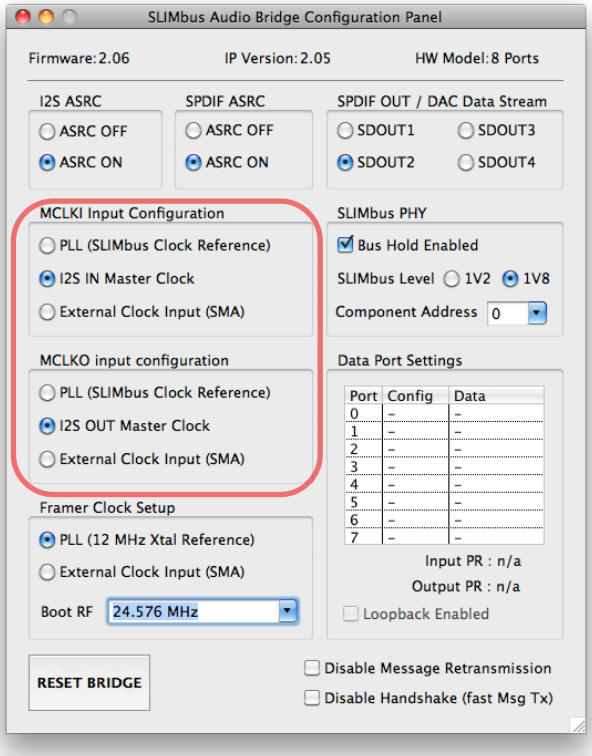
- Press the knob to access the possible values for the parameter and select "**DSI IN Master Clk**" by rotating the knob.



- Press the knob to validate the new setting.

The bridge will now take its input (output) audio master clock from the DSIO interface.

Bridge Control Panel:
In the software, got to the menu "**Tools**" and select the submenu "**Bridge Control Panel**". Select the "**I2S IN Master clock**" (or "**I2S OUT Master Clock**") in the "MCLKx Input Configuration box".


SLIMbus Audio Bridge Configuration Panel
Firmware: 2.06
IP Version: 2.05
HW Model: 8 Ports
I2S ASRC
ASRC OFF
ASRC ON
SPDIF ASRC
ASRC OFF
ASRC ON
SPDIF OUT / DAC Data Stream
SDOUT1
SDOUT3
SDOUT2
SDOUT4
MCLKI Input Configuration
PLL (SLIMbus Clock Reference)
I2S IN Master Clock
External Clock Input (SMA)
SLIMbus PHY
Bus Hold Enabled
SLIMbus Level 1V2 1V8
Component Address 0
MCLKO input configuration
PLL (SLIMbus Clock Reference)
I2S OUT Master Clock
External Clock Input (SMA)
Data Port Settings
Port Config Data
0 – –
1 – –
2 – –
3 – –
4 – –
5 – –
6 – –
7 – –
Input PR : n/a
Output PR : n/a
Loopback Enabled
Framer Clock Setup
PLL (12 MHz Xtal Reference)
External Clock Input (SMA)
Boot RF 24.576 MHz
RESET BRIDGE
Disable Message Retransmission
Disable Handshake (fast Msg Tx)