# Lnk

# AN-005 APPLICATION NOTE

# **AP PSIA Setup**

for optimal operation with the LnK SLIMbus Audio Bridge



LnK 44, rue des Combattants B-4624 Romsée Belgium <u>www.lnk-tools.com</u> info@Ink-tools.com

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### **1. Purpose of the document**

This document will guide the user through the setup of the Audio Precision PSIA transmitter and receiver.

A basic knowledge of the operation of the SLIMbus Audio Bridge and the PSIA is required to follow the various explanations given in this document. Refer to the SLIMbus Audio Bridge HW and SW user manuals, the APWIN (or AP2700) user manual and the PSIA datasheet for more information about these equipments.

The LnK SLIMbus Bridge is used to inject or receive digital audio on SLIMbus. It allows the PSIA 2722 to directly feed a digital signal to a SLIMbus audio device and / or to receive and analyze a digital audio signal coming from a SLIMbus audio device.



The PSIA Transmitter is connected to the bridge DSIO (I2S) input. The PSIA Receiver is connected to the bridge DSIO (I2S) output.

| PSIA Signal           | Audio Bridge DSIO signal     |
|-----------------------|------------------------------|
| MASTER CLK (optional) | МСК                          |
| BIT CLK               | ВСК                          |
| FRAME CLK             | LRCK                         |
| DATA                  | SD1 (SD2 to SD4 also usable) |

## 3. PSIA Transmitter Setup

The DSIO (I2S) input of the LnK SLIMbus Audio Bridge is **slave**. This means that it must receive the bit clock and the word clock from the PSIA. Therefore, the Frame and Bit clock direction shall be set to "**Out**".

| 💦 PSIA Serial In                  | terface T          | ransmit             | tter       |           |                     |              |                 |
|-----------------------------------|--------------------|---------------------|------------|-----------|---------------------|--------------|-----------------|
| Channel Data Assi                 | gnment             |                     |            |           | Channel Da          | ta Structure |                 |
| Generator Channe                  | I A                | В                   |            | 0         |                     |              | > 31            |
| Data Channel                      | 0                  | 1                   |            |           | MSB Fi              | ist 🗹        |                 |
| I2S Loop                          | p-Back R           | ise / Fall          |            | Pad       | Dat                 | a            | Pad             |
| Transmit Data Cloc                | sk 🔇               | $\odot$             |            | 0 6       | its 24 L            | inear 🔽      | 8 bits          |
| PreEmphasis: 0                    | ff                 | *                   |            | High      | L Jus               | iify R       | Low 🚩           |
| Scale Freq. By: O                 | utput Rate (       | SR) 🔽               |            |           |                     |              |                 |
| Rate Ref: 48                      | 3.0000 kHz         |                     |            |           |                     |              |                 |
|                                   |                    | Bit Cloc            | ∙k         | Shift Bit |                     |              |                 |
| Clocks                            | Direction          | Edge Sy<br>Bise / F | inc Invert | 1 bit Wid | e<br>Callina        | С            | omputed<br>Bate |
| Frame Clock (Fs)<br>(Word Clock)  | • •                | 0 0                 |            |           | 48.0000 kHz         | = 48.00      | 00 kHz          |
| Channel Clock<br>(Subframe Clock) | OUT                | 0 0                 |            |           | x 2 chan            | nels = 96.00 | 00 kHz          |
| Bit Clock                         | $\odot$ $\bigcirc$ |                     |            |           | x 32 bits/<br>chann | nel = 3.072  | 00 MHz          |
| N*Fs                              | OUT                |                     |            |           | 256 x Fs            | = 12.28      | 80 MHz          |
| Master Clock Tx Out               |                    | Rx In 🔽             | ]          |           | x Fs                | = 12.28      | 80 MHz          |
| Logic Voltage Level               |                    |                     |            |           |                     |              |                 |
| 5V 3.3V 3.3V 2.4V 1.8V            |                    |                     |            |           |                     |              |                 |
| Uutputs                           | J                  |                     |            | 01        |                     |              |                 |
|                                   |                    |                     |            | TTL       | CMOS                |              |                 |

The serial data format of the bridge is Left Justified. Therefore, there is no bit shift like in the PHILIPS I2S format. The channel data structure shall be set to "**MSB first**". The sample length can take any value till 24 bits. The bridge inputs or outputs frames of 64 bits (32 bits per channel).

The Bit Clock Edge Sync shall be set to "**Fall**". The Word Frame (Wfm) shall be **inverted**.

The "Logic Voltage Level" (signaling voltage) must be set to "CMOS 3.3V".

Make sure that the PSIA transmitter outputs are "ON".

#### 4. PSIA Receiver Setup

The I2S output of the LnK SLIMbus Audio Bridge is **master**. This means that it will transmit the bit clock and the word clock to the PSIA. Therefore, theFrame and Bit clock direction shall be set to "**In**".

| हे PSIA Serial Int                | terface R             | eceive              | r                      |               |               |                       |                  |                 |
|-----------------------------------|-----------------------|---------------------|------------------------|---------------|---------------|-----------------------|------------------|-----------------|
| Channel Data Assig                | gnment                |                     |                        |               |               | Channel Data          | Structure        |                 |
| Analyzer Channel                  | A                     | В                   |                        | 0             |               |                       |                  | > 31            |
| Data Channel                      | 0                     | 1                   |                        |               |               | MSB First             | <b>V</b>         |                 |
| 125                               | B                     | ise / Fall          |                        |               | Pad           | Data                  |                  | Pad             |
| Receive Data Cloc                 | k (                   | ) ()                |                        | 0             | bits          | 24 Bits               | ~                | 8 bits          |
| DeEmphasis: Of                    | f                     | ~                   |                        |               |               | L Justify             | R                |                 |
| Scale Freq. By: Me                | eas Input R           | ate 🗸               |                        | A:            | 24            | 20 16 12              | : 8<br><b></b> - | 4               |
| Rate Ref: 48                      | .0000 kHz             |                     |                        | В:            |               | Active Bits           | Data B           |                 |
|                                   |                       | Dit Clas            | -                      | CLiA          | D3            |                       | U D did D        |                 |
| Clocks                            | Direction<br>Out / In | Edge Sy<br>Rise / F | ync Invert<br>Fall Wfm | 1 bit<br>left | Wide<br>Pulse | Setting               | C                | omputed<br>Rate |
| Frame Clock (Fs)<br>(Word Clock)  | 0 0                   | 0 0                 | •                      |               |               | 48.0000 kHz           | = 48.00          | 00 kHz          |
| Channel Clock<br>(Subframe Clock) | OUT                   | 0 (                 | •                      |               |               | x 2 channel           | s = 96.00        | 00 kHz          |
| Bit Clock                         | $\odot$ $\odot$       |                     |                        |               |               | x 32 bits/<br>channel | = 3.072          | 00 MHz          |
| N×Fs                              | OUT                   |                     |                        |               |               | 256 x Fs              | = 12.28          | 80 MHz          |
| Master Clock                      | Tx Out, I             | Rx In 🔽             |                        |               |               | 256 x Fs              | = 12.28          | 80 MHz          |
|                                   |                       |                     | Logic V                | oltage        | Level         |                       |                  |                 |
| 5V 3.3V 3.3V 2.4V 1.8V            |                       |                     |                        |               |               |                       |                  |                 |
| Uutputs                           | J                     |                     |                        |               |               |                       |                  |                 |
|                                   |                       |                     |                        | TTL           |               | СМОЗ                  | <u> </u>         |                 |

The serial data format of the bridge is Left Justified. Therefore, there is no bit shift like in the PHILIPS I2S format. The channel data structure shall be set to "**MSB first**". The sample length can take any value till 24 bits. The bridge inputs or outputs frames of 64 bits (32 bits per channel).

The Bit Clock Edge Sync shall be set to "**Fall**". The Word Frame (Wfm) shall be **inverted**.

The "Logic Voltage Level" (signaling voltage) must be set to "CMOS 3.3V".

Make sure that the PSIA transmitter outputs are "**ON**" if the PSIA Master Clock has to be used. Otherwise set it to "**OFF**".

### 5. Bridge Clock Input Selection

The SLIMbus Audio Bridge clock source selector can be set by using the bridge configuration menu itself or via the PC control software.

#### Bridge configuration menu:

- Press the rotary knob.
- Rotate the knob to reach "Select MCLKI src" or "Select MCLKO src".

Fxit. >Select MCLKI < src Select MCLKO src Set DSI IN ASRC Set S/PDIF IN ASRC Select DAC stream Select Framer Clk Set Framer BootRF Set Framer BootMod Set Comp. Address Set SLIMbus Level Set Bus Hold Fxit.

- Press the knob to access the possible values for the parameter and select "DSI IN Master CIk" by rotating the knob.

MCLKI Clock Source PLL (SLIMbus ref) >DSI IN Master Clk ( External Clk (SMA)

- Press the knob to validate the new setting.

The bridge will now take its input (output) audio master clock from the DSIO interface.

#### Bridge Control Panel:

In the software, got to the menu "Tools" and select the submenu "Bridge Control Panel". Select the "I2S IN Master clock" (or "I2S OUT Master Clock") in the "MCLKx Input Configuration box".

| 😶 🔿 💽            | LIMbus Audio Bridge Con | figuration Pane  | 1                 |  |  |
|------------------|-------------------------|--|-------------------|--|--|
| Firmware: 2.06   | IP Version: 2.05        | HW   | Model:8 Ports     |  |  |
| I2S ASRC         | SPDIF ASRC              | SPDIF OUT / D  | AC Data Stream    |  |  |
| O ASRC OFF       | O ASRC OFF              | ⊖ SDOUT1   | ⊖ SDOUT3          |  |  |
| ASRC ON          | ASRC ON                 | SDOUT2   | ⊖ SDOUT4          |  |  |
| MCLKI Input Cor  | figuration              | SLIMbus PHY  |                   |  |  |
| OPLL (SLIMbus    | Clock Reference)        | 🗹 Bus Hold En  | abled             |  |  |
| • I2S IN Master  | Clock                   | SLIMbus Level () 1V2 () 1V8<br>Component Address () ()<br>Data Port Settings |                   |  |  |
| O External Cloc  | k Input (SMA)           |  |                   |  |  |
| MCLKO input co   | nfiguration             |  |                   |  |  |
| OPLL (SLIMbus    | Clock Reference)        | Port Config  | Data              |  |  |
| I2S OUT Mast     | er Clock                | 0 -  |                   |  |  |
| External Cloc    | k Input (SMA)           | 2 -  | -                 |  |  |
| 0                |                         | <u> </u>   | -                 |  |  |
| Framer Clock Set | tup                     | 5 -  | -                 |  |  |
| • PLL (12 MHz )  | Ktal Reference)         | 7 -  | -                 |  |  |
| External Clock   | k Input (SMA)           | In   | put PR : n/a      |  |  |
|                  |                         | Out  | put PR : n/a      |  |  |
| Boot RF 24.57    | 6 MHz                   | Loopback I   | Enabled           |  |  |
|                  |                         | )isable Message  | Retransmission    |  |  |
| RESET BRIDGE     |                         | Jisable Handeba  | ke (fast Mcc Ty   |  |  |
|                  |                         | isable natiusta  | ike (last wisg TX |  |  |