SLIMbus Audio Bridge User Manual

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1. Presentation of the tool

The SLIMbus Audio Bridge makes the link between SLIMbus and the SPDIF or the DSI (Digital Serial Interface) legacy audio interfaces.

The main purpose of the bridge is to allow easy tests of audio capabilities of a SLIMbus component with traditional audio analyzers (Audio Precision, Rhode&Swartz ...).

The bridge is also a fully featured and compliant SLIMbus component. It can be used to test other SLIMbus components (especially SLIMbus Manager or other audio components).

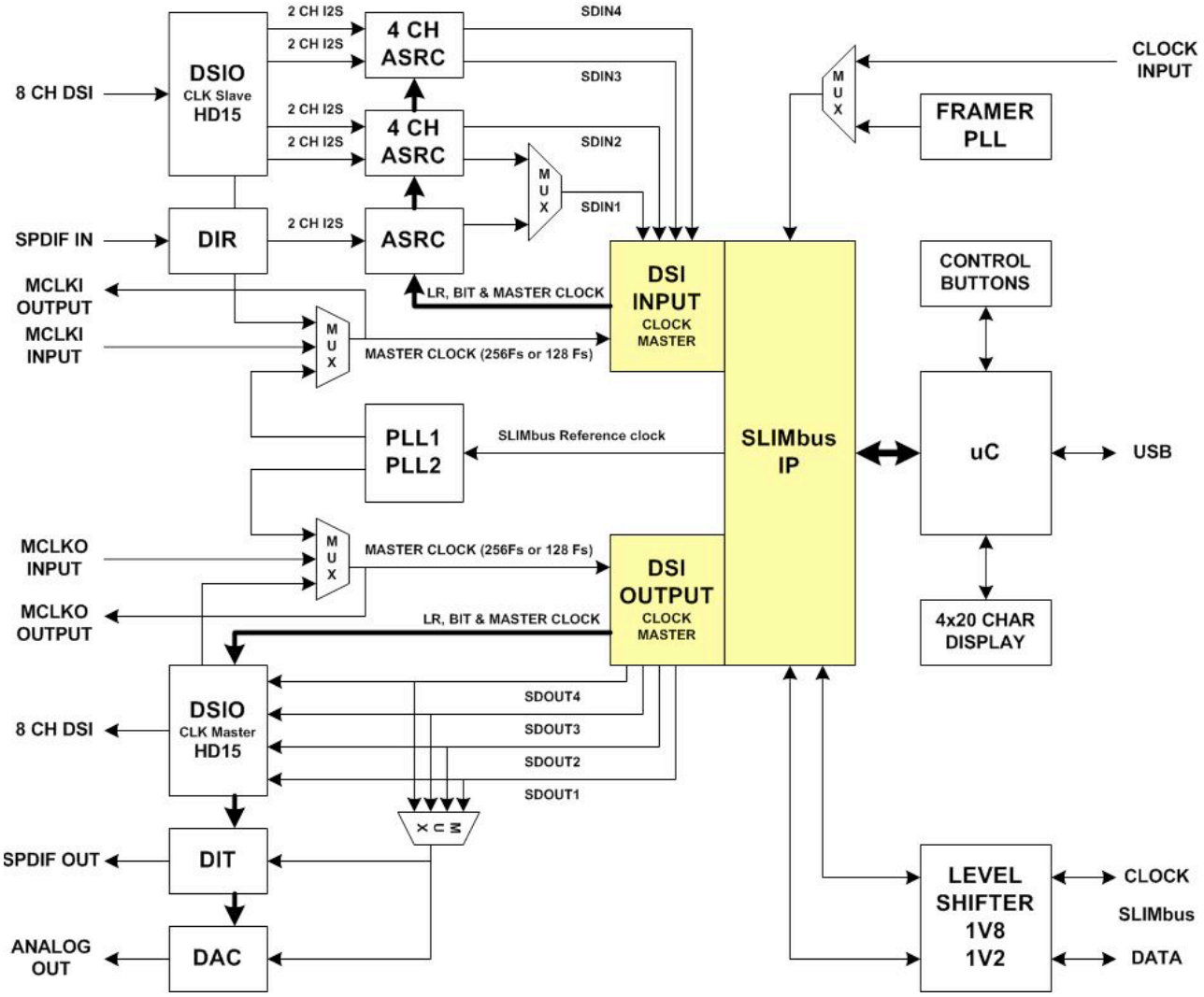
Features:
- 2 or 8 data ports (depending on the model)
- 1 or 4 DSI input streams on HD15 connector (VGA type) sharing the same bit clock (BCLK) and word clock (LRCLK)
- 1 or 4 DSI output streams on HD15 connector (VGA type) sharing the same bit clock (BCLK) and word clock (LRCLK)
- SPDIF input and output
- Analogue output (stereo)
- Data loop back function
- Very flexible clock management

The data ports must operate by pair and can be source or sink. Additionally, all sink ports must use the same Presence Rate. Similarly, all the source must use the same presence rate. Note that the channel rates must not necessarily be identical. The transport protocols can also differ. Only the Presence Rate does matter.

Port	DSI Ch	As source, mapped to	As sink, mapped to
0	B	S/PDIF stream or DSI Input stream 1	DSI Output stream 1
1	A		
2	B	DSI Input stream 2	DSI Output stream 2
3	A		
4	B	DSI Input stream 3	DSI Output stream 3
5	A		
6	B	DSI Input stream 4	DSI Output stream 4
7	A		

The S/PDIF output and the analogue output can use the DSI Output stream 1 to 4 (user selectable).

The following figure shows a high level diagram of the bridge architecture. The SLIMbus interface specificities are not shown here and the SLIMbus IP is treated as a black box.



SLIMbus Enumeration Address

Component address = 0

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0001	0x00	0x00	**0x01C100010000**
Framer	0x01C1	0x0001	0x01	0x00	**0x01C100010100**
Generic	0x01C1	0x0001	0x02	0x00	**0x01C100010200**

Component address = 1

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0001	0x00	0x01	**0x01C100010001**
Framer	0x01C1	0x0001	0x01	0x01	**0x01C100010101**
Generic	0x01C1	0x0001	0x02	0x01	**0x01C100010201**

2. Using the tool

The bridge is a stand alone device. It has its own alphanumerical display (4 lines of 20 characters) and controls (rotary encoders with push button) for the required parameter changes.

2.1. Display Pages

The bridge status and configuration is spread over 8 pages, by themes:
- Main page: Signal routing, Port status, presence rate and error reporting
- Page 1: Audio Input Clock
- Page 2: Audio Output Clock
- Page 3: Bus Clock configuration
- Page 4: Framer Status
- Page 5: SLIMbus PHY configuration
- Page 6: Bridge Value Elements
- Page 7: Product Info

The page navigation is simply done by turning left or right the button.

2.1.1. Main Page

This page summarize the important operational information.

```
 DSI  >ASRC24>SB>------
P01234567 OPR=n/a
 II------- IPR=48k
Framer:Off,RF=1
```

The first line indicates the digital audio input source (DSI or SPDIF), the signal processing (**A**synchronous **S**ample **R**ate **C**onverter or Direct) followed by the sample length (in bit) and the output stream selected for playback on the analogue output and the SPDIF output.

The input source selection is automatic. The bridge detects if there is a valid stream on the SPDIF input and switch to it. The automatic input selection only works when there is a SLIMbus clock present on the bridge and that there are at least 1 data port set as a source. Note that the SPDIF data are only streamed to the Ports 0 and 1.

When the bridge is powered ON, the first line shows:

```
-------->-------->SB>------
```

When one of the data ports is configured as a source, the first line will show the active input and the processing that is done on the signal before it is sent on SLIMbus.

```
SPDIF>ASRC24>SB>------
SPDIF>Direct>SB>------
 DSI  >ASRC16>SB>------
 DSI  >Direct>SB>------
```

When one of the data ports is configured as a sink, the first line will show which of the 4 DSI streams that is used by the analogue output and the SPDIF output.

```
--------->-------->SB>SD01
--------->-------->SB>SD02
--------->-------->SB>SD03
--------->-------->SB>SD04
```

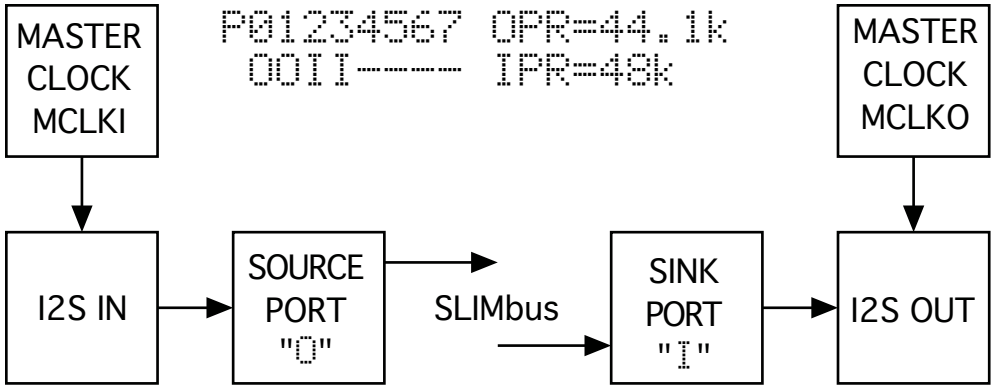
If both the source and sink ports are configured an are operational, the line will show the complete signal path. For instance:

```
SPDIF>ASRC20>SB>SD02
```

The second and third lines are showing the port status (connected as source or connected as sink) and the presence rate of the sink ports (IPR) and the source ports (OPR).
When a port is not configured, its status is shown with a "-". When a port is configured as **sink** (input data from SLIMbus) and a valid reconfiguration defined the channel structure and content, its status is shown with a "I". When a port is configured as **source** (output data to SLIMbus) and a valid reconfiguration defined the channel structure and content, its status is shown with a "O".
The input and output presence rate are also shown when applicable. If for any reason a mismatch was detected in the presence rate of all the sink ports or all the source ports, the display will show "ERROR" instead of a presence rate value.

The following examples shows 4 configured ports. Ports 0 and 1 are configured as source ports (they output data on SLIMbus) and they have an output presence rate (OPR) equal to 44,1kHz. Ports 2 and 3 are configured as sink port (they read data from SLIMbus) and they have an input presence rate equal to 48kHz.

```
P01234567 OPR=44.1k
  OOII----  IPR=48k
```



Note: When the audio master clock is generated by the PLL and the frequency is not exactly what is displayed, the "=" sign becomes "#". This could be the case when the root frequency is 24 MHz and the presence rate is equal to 44.1kHz (other Root Frequency / Presence Rate combination can lead to errors - see the Annex B for more information). The master clock error is 126Hz, leading to a sample clock error of 0.49Hz. Not much but worthwhile to mention...

```
P01234567 OPR#44.1k
  OOII----  IPR=48k
```

The forth line of the page displays the bridge status. In case of no error, the display shows the Framer status summary (Primary/Inactive, Root Frequency and clock source).

```
Framer:Off,RF=1
Framer:Ena,RF=1(PLL)
Framer:Ena,RF=1(SMA)
```

Note that the Framer status line shows the actual status of the Framer, not the desired status following a power on or a reset. If the status of the Framer is changed from Inactive to Primary by modifying the bridge parameters, this will not affect the framer status which will keep showing “Off”. It is only after a reset or a power cycle (OFF/ON) that the new status will take effect (“Ena”) and will be displayed on the main page.

If there is an error condition, the last line shows the reason of the problem and hide the framer status.

2.1.2. Audio Input Clock

This page shows the configuration of the master clock of the DSI input interface.
For sample rate lower than 128 kHz, the oversampling ration is equal to 256. For 128kHz and above, the oversampling ration is equal to 128.

```
1. Audio Input Clk
MCLKI Src: DSI IN
Freq: 12288.000 kHz
Ferr: n/a    ,CGmin=-
```

The second line of the page sows the source of the master clock. It can either be PLL generated, input from the DSI IN connector or input from SMA connector. See the clock management section for more detailed information.

The third line shows the actual frequency of the clock. Note that the frequency displayed is only guarantied in PLL mode. The bridge does not have a frequency meter. When the source is either DSI or SMA, the value indicates the required clock frequency. It is the responsibility of the user to provide the right frequency.

When generated by the PLL, the forth line shows the frequency error compared to ideal value and the clock gear down to which the bridge can operate.

2.1.3. Audio Output Clock

This page shows the configuration of the master clock of the DSI output interface.
For sample rate lower than 128 kHz, the oversampling ratio is equal to 256. For 128kHz and above, the oversampling ratio is equal to 128.

```
2. Audio Output Clk
MCLKO Src: PLL
Freq: 11289.474 kHz
Ferr: 126 Hz,CGmin=6
```

The second line of the page sows the source of the master clock. It can either be PLL generated, input from the DSI OUT connector or input from SMA connector. See the clock management section for more detailed information.

The third line shows the actual frequency of the clock. Note that the frequency displayed is only guarantied in PLL mode. The bridge does not have a frequency meter. When the source is either DSI or SMA, the value indicates the required clock frequency. It is the responsibility of the user to provide the right frequency.

When generated by the PLL, the forth line shows the frequency error compared to ideal value and the clock gear down to which the bridge can operate.

2.1.4. Bus Clock Configuration

This page shows the SLIMbus clock configuration (Clock Gear and Root Frequency).

```
3. Bus CLock Config
CG:9 (6.4 - 14.4MHz)
RF:1 (24.576 MHz)
Bus Clock:12.288 MHz
```

The actual bus clock is computed based on the Root Frequency and Clock Gear values.

2.1.5. Framer Status

The bridge features a Framer that can be active or inactive.

```
4. Framer Status
Boot Mode: Inactive
Clock Source: PLL
Boot RF: 19.200 MHz
```

Boot mode indicate how the framer will behave at boot time. It can be Inactive or Primary. The framer accepts it clock from an on board PLL or from an external clock source (SMA connector).
Boot RF sets the PLL if it used as a source and indicate to the framer what to write in the Framing Information bits.

2.1.6. SLIMbus PHY

The bridge features a Framer that can be active or inactive.

```
5. SLIMbus PHY
Bus Holder   : On
SLIMbus Level: 1.8 V
Comp. Address: 0
```

Bus Holder indicates the status of the bus hold on the data line. It can be activated (On) or deactivated (Off).
SLIMbus level shows the voltage used on the SLIMbus IO. It can be either 1.8V or 1.2V.
Comp Address is the Instance Value of the bridge. It can be equal to 0 or 1. It allows two bridges to operate on the same SLIMbus.

2.1.7. Value Elements

The bridge features 3 Value Elements, attached to the Generic Device. The bits of each VE has a specific function (see section 6.2 form more detailed information).
They can be programmed through SLIMbus. The page shows the value they have been assigned. If the VE value has an effect on the bridge, some deoded values or parameters are shown after the value of the VE.

```
6. Value Elements
VE0=0
VE1=0
VE2=130 --,SD02,0dB
```

2.1.8. Product Information

The last page displays the product ID, the firmware revision of the SLIMbus IP and the controller code.

```
7. Product Info
Model : 8P bridge
FW Rev.: 2.00
IP Rev.: 2.00
```

2.2. Changing Parameters

By pressing the button, the bridge will enter in the parameter edition menu. Navigate in the item list by rotating the button to the left or the right.

```
>Exit                    <
 Select MCLKI src
 Select MCLKI src
 Set DSI IN ASRC
 Set S/PDIF IN ASRC
 Select DAC stream
 Select Framer Clk
 Set Framer BootRF
 Set Framer BootMod
 Set Comp. Address
 Set SLIMbus Level
 Set Bus Hold
 Exit
```

There are 11 parameters that can be modified. The selected item is enclosed by the “>” and “<“ signs.
When the desired parameter is selected, press on the button to access the list of the possible values of that particular parameter.

For instance, to select the MCLKI source, go to "Select MCLKI src" and press the button. The display will show:

```
MCLKI Clock Source
>PLL (SLIMbus ref) <
 DSI IN Master Clk
 External Clk (SMA)
```

The selected item is enclosed by the ">" and "<" signs. Navigate in the parameter value by rotating the button to the left or the right. Press the button to validate the selected value. At that moment, the display goes back to the parameter list.

To exit the parameter edition, move the cursor to Exit and press the button. The display will show the last displayed information page.

Parameter Item	Parameter Values
Select MCLKI src	PLL (SLIMbus ref) DSI IN Master Clk External Clk (SMA)
Select MCLKO src	PLL (SLIMbus ref) DSI OUT Master Clk External Clk (SMA)
Set DSI IN ASRC	Disabled Enabled
Set S/PDIF IN ASRC	Disabled Enabled
Select DAC stream	SDO1 (Ports 0 & 1) SDO2 (Ports 2 & 3) SDO3 (Ports 4 & 5) SDO4 (Ports 6 & 7)
Select Framer Clk	PLL (12MHz ref) External Clk (SMA)
Set Framer BootRF	??.??? MHz (RF=0) 24.576 MHz (RF=1) 22.5792MHz (RF=2) 15.360 MHz (RF=3) 16.800 MHz (RF=4) 19.200 MHz (RF=5) 24.000 MHz (RF=6) 25.000 MHz (RF=7) 26.000 MHz (RF=8) 27.000 MHz (RF=9)
Set Framer BootMod	Inactive Primary
Set Comp. Address	Instance Value 0 Instance Value 1
Set SLIMbus Level	IO Voltage: 1.2V IO Voltage: 1.8V
Set Bus Hold	Bus Hold Disabled Bus Hold Enabled

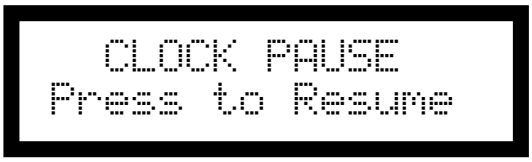
2.3. Resetting the bridge

To reset the bridge while it is in operation, press the button for at least 4 seconds and release it. The controller will reboot and the SLIMbus interface will be hard reset. The bridge reset is similar to a power ON.

Use the bridge reset when the Framer boot mode, the Framer Boor Root Frequency or the component address is modified and must take effect.

2.4. SLIMbus Clock Wake Up

When a SLIMbus reconfiguration sequence pauses the SLIMbus clock, the bridge display will show:



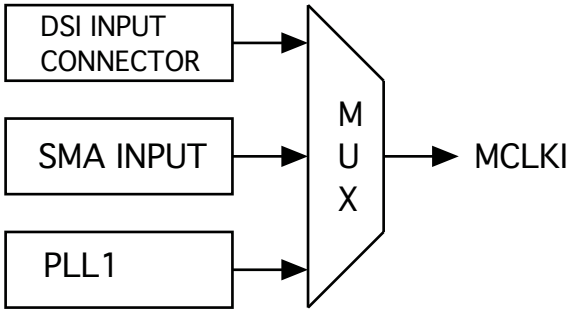
Press the rotary knob to toggle the SLIMbus data line and force the framer to resume clock operation.

3. Clock Management

The bridge has a powerful and flexible clock management scheme.

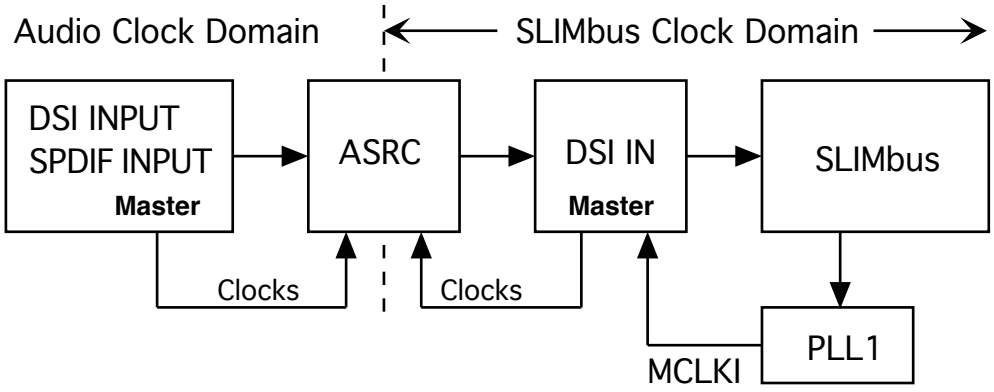
3.1. DSI Input Master Clock (MCLKI)

The digital audio input master clock (MCLKI) can be generated by a PLL using the SLIMbus clock as reference or input from the DSI connector or the SMA connector.



The MCLKI clock is buffered and output on a SMA connector to eventually synchronize other audio devices or measurement tools.

An asynchronous sample rate converter (ASRC) is available on the SPDIF and DSI inputs to prevent eventual issues linked to the crossing of 2 different clock domains (digital audio / SLIMbus). The 2 clocks might not have any relationship, which could lead to data loss. The ASRC is the bridge between the 2 clock domains and is of such a high quality that the measured performances of the device under test will not be affected by the ASRC.

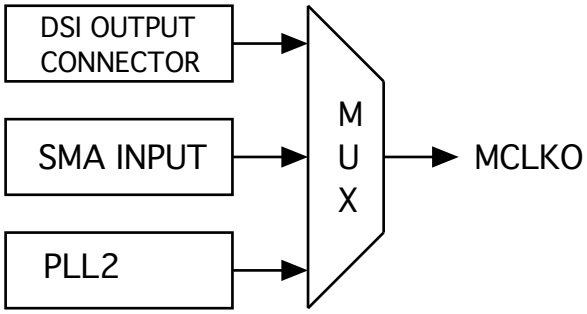


The device feeding the DSI input signals into the bridge must be the **clock master**. It must provide the bit clock and the word clock to the bridge. The master clock (at 128Fs or 256Fs) can be used as reference master clock (MCLKI) when selected by the feeding device.

If the PLL operation mode is not selected, the user is free to feed the bridge with its own MCLKI clock. Depending on the complete setup clock structure and the transport protocols in use, the user will activate or deactivate the ASRC.

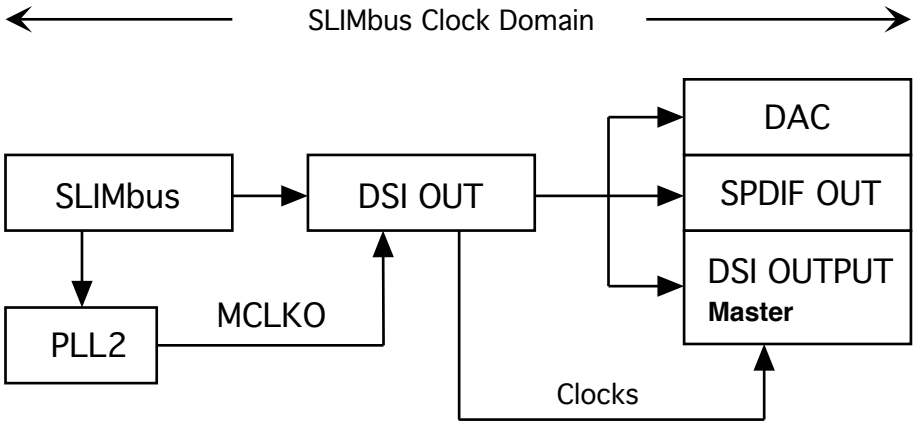
3.2. DSI Output Master Clock (MCLKO)

The digital audio input master clock (MCLKI) can be generated by a PLL using the SLIMbus clock as reference or input from the DSI output connector or the SMA connector.



The MCLKO clock is buffered and output on a SMA connector to eventually synchronize other audio devices or measurement tools.

When using the PLL, the DSI or SPDIF outputs do not need an asynchronous sample rate converter as their clocks are derived from the SLIMbus clock. There is no clock domain crossing in this case.



If the PLL operation mode is not selected, the user is free to feed the bridge with its own MCLKO clock. In this case, the SLIMbus clock domain stops at the DSI OUT interface of the SLIMbus IP. It is the responsibility of the user to ensure that the clock structure of the complete setup is suitable for an error free transmission of the audio samples.

3.3. Concurrent use of PLL generated MCLKI and MCLKO

As PLL1 and PLL2 are sharing the same SLIMbus reference clock, there are some limitations in the combinations of Root Frequency / Input Presence Rate / Output Presence Rate.

The SLIMbus reference frequency is stable across the clock gear. But its actual value depends on the desired Presence rate and the Root frequency in use.
It is ranging from Gear 6 to Gear 9. This means that if the reference frequency is equal to clock gear 6, the bridge will not allow audio streaming with a clock gear below 6.
Due to inherent PLL limitations, the required reference clock for the input presence rate might be different than the required reference clock for the output presence rate. In this case, concurrent operation of PLL1 and PLL2 is not possible and the bridge displays an

error message in the status line of the main page. See Annex A for the allowed combinations for a given Root Frequency.

3.4. Framer Clock Source

When the Framer of the bridge is active, it can receive its clock from a PLL or from an external clock source.

Root Frequency	PLL Generated	Externally Fed
RF=0 (“Not Indicated”)	Not Possible	Any frequency
RF=1 (24,576 MHz)	24,576 MHz	24,576 MHz
RF=2 (22,5792 MHz)	22.578998 MHz (Error of -202 Hz)	22,5792 MHz
RF=3 (15,36 MHz)	15,36 MHz	15,36 MHz
RF=4 (16,8 MHz)	16,8 MHz	16,8 MHz
RF=5 (19,2 MHz)	19,2 MHz	19,2 MHz
RF=6 (24 MHz)	24 MHz	24 MHz
RF=7 (25 MHz)	25 MHz	25 MHz
RF=8 (26 MHz)	26 MHz	26 MHz
RF=9 (27 MHz)	27 MHz	27 MHz

For proper operation of the audio master clock PLLs, the Root Frequency must be accurately set according to the SLIMbus specification and its value must be entered in the bridge (Framer BootRF parameter).

4. Error Cases

The bridge will display an error message when proper operation is not achieved.
There could be many reasons why audio streaming would not be effective.

4.1. Input Presence Rate Mismatch

The sink ports are all sharing the same DSI clocks (MCLKO reference). Therefore, they must also use the same Presence Rate.
When 2 or more sink ports are not getting assigned the same Presence Rate, the bridge will report an error and will not setup any data transmission. The error is shown on the display main page.

```
 DSI >ASRC24>SB>------
P01234567 OPR=n/a
 II------- IPR=Error
Err: IPR mismatch...
```

To solve the problem, assign the proper Presence rate to the data channels attached to the sink ports.

4.2. Output Presence Rate Mismatch

The source ports are all sharing the same DSI clocks (MCLKI reference). Therefore, they must also use the same Presence Rate.
When 2 or more source ports are not getting assigned the same Presence Rate, the bridge will report an error and will not setup any data reception. The error is shown on the display main page.

```
 DSI >ASRC24>SB>SDO2
P01234567 OPR=Error
 --OO----- IPR=n/a
Err: OPR mismatch...
```

To solve the problem, assign the proper Presence rate to the data channels attached to the source ports.

4.3. Incompatible Input and Output Presence Rate

The Presence Rate incompatibility error only happens when the PLL operation is selected. When the Input Presence Rate and the Output Presence Rate are leading to conflicting PLL settings, the “!” symbol is displayed after OPR and IPR to indicate that the PLL could not be set.

```
 DSI >ASRC24>SB>SDO2
P01234567 OPR!192k
 IIOO----- IPR!48k
Err: Incompatible PR
```

Running on external clocks will not have such limitations.

Another cause of Presence Rate mismatch is due to the required oversampling ratio.
When the Presence Rate is equal or greater than 128 kHz, the master clock is set to 128Fs. It is set to 256Fs for the other presence rates.

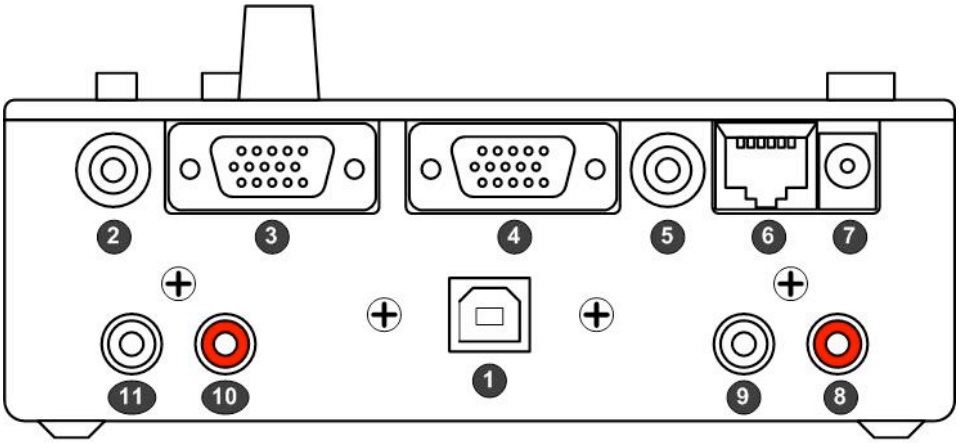
The oversampling ratio applies to both the DSI input and output interfaces. This means that when using such high sampling rates, it must be used on every active channels.
This applies to both PLL and external clock operation.

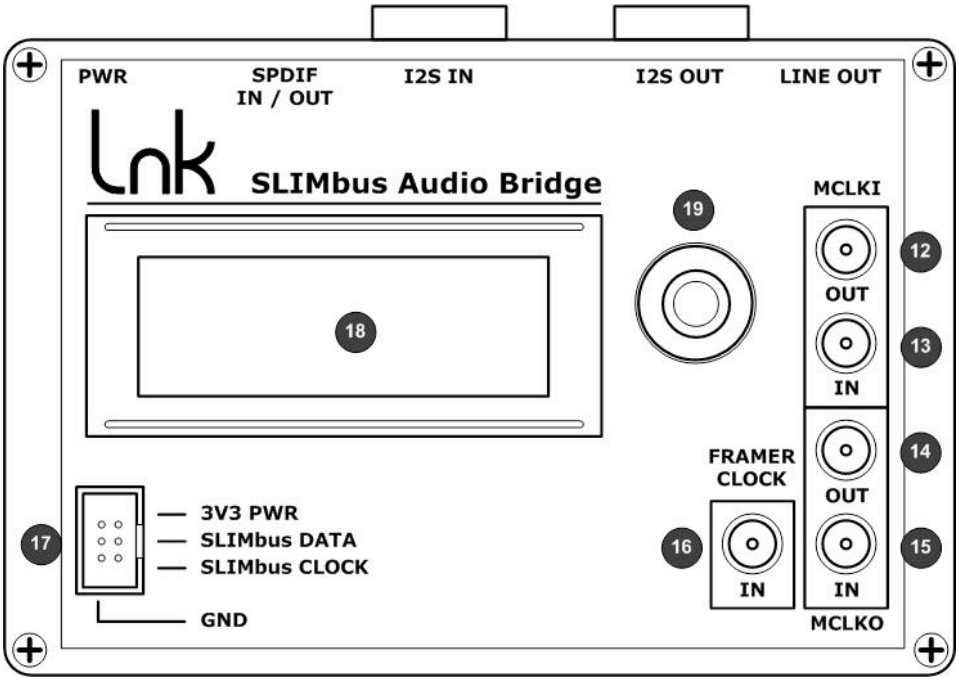
4.4. Incompatible Clock Gear

The Clock Gear incompatibility only happens when the PLL operation is selected. When the Clock Gear is too low to allow proper PLL operation, the "!" symbol is displayed after OPR and IPR to indicate that the PLL could not be set.

Running on external clocks will not have such limitations. However, the clock gear must be such that there is enough bandwidth in the SLIMbus to fit the desired data channels.

5. Bridge Connectivity





1. USB connector	2. Line out stereo jack	3. HD15 DSI output	4. HD15 DSI input
5. SPDIF in/out jack	6. Service connector	7. DC Power input	8. SPDIF OUT
9. SPDIF IN	10. Line out - Right	11. Line out - Left	12. DSI IN MCLK IN
13. DSI IN MCLK OUT	14. DSI OUT MCLK IN	15. DSI OUT MCLK OUT	16. FRAMER CLOCK IN

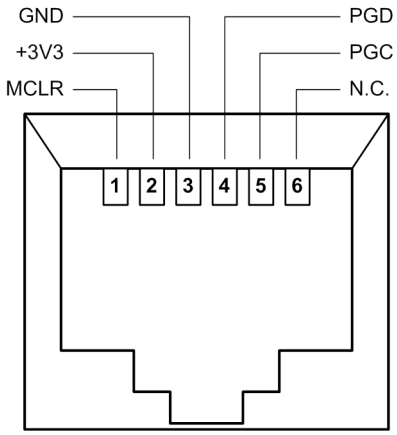
5.1. DC Supply Barrel Jack

This is the power supply connector of the bridge.

Signal Name	Pin Number	Function	
VDD (7V to 12V)	Center pin	Input	
GND	Outer ring	Ground	

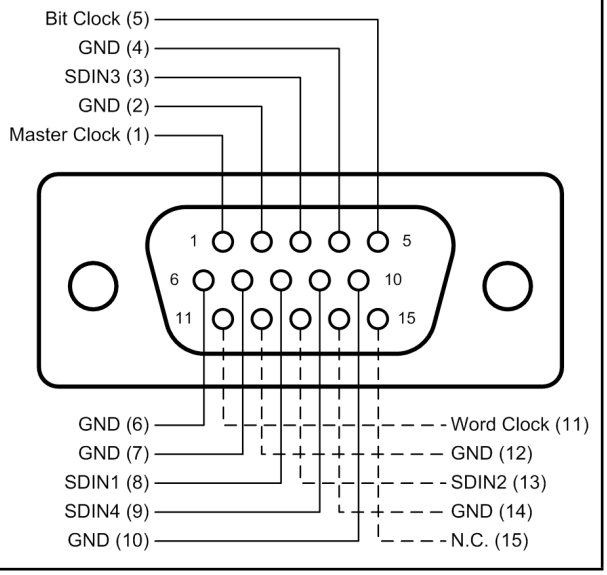
5.2. Service Modular Jack

This RJ11 connector give access to the bridge controller for eventual firmware upgrades.

Signal Name	Pin Number	Function	
MCLR	1	Input	
+3V3	2	Power	
GND	3	Ground	
PGD - Serial Data	4	Bidir	
PGC - Serial clock	5	Input	
Not Connected	6		

5.3. DSI Input HD15 Connector

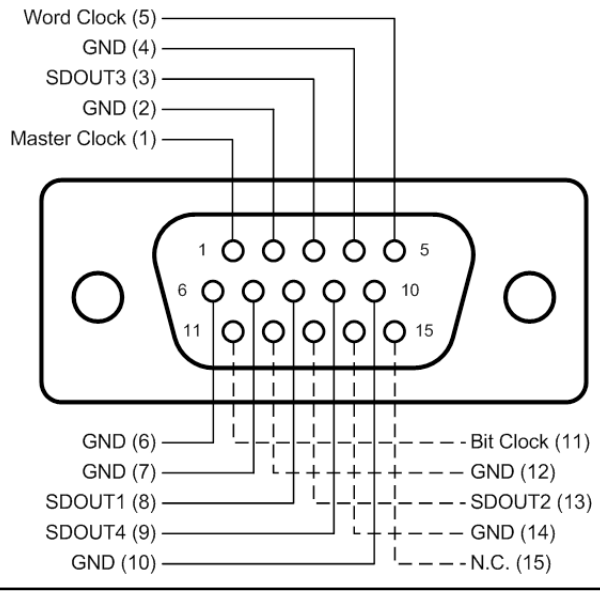
The DSI input interface is mapped on a HD15 male connector.

Signal Name	Pin Number	Function	
Master Clock (MCLK)	1	Input	
Word Clock (LRCLK)	11	Input	
Bit Clock (BCLK)	5	Input	
SDIN1	8	Input	
SDIN2	13	Input	
SDIN3	3	Input	
SDIN4	9	Input	
GND	2, 4, 6, 7, 10, 12, 14	Ground	

The nominal signal level is equal to 3.3V. Maximum input level is 3.6V. Note that Bit clock and word clocks are on different pins than on the DSI OUT connector.

5.4. DSI Output HD15 Connector

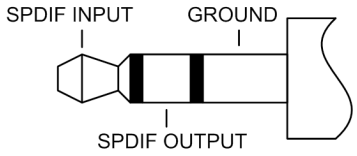
The DSI Output interface is mapped on a HD15 male connector.

Signal Name	Pin Number	Function	
Master Clock (MCLK)	1	Input	
Word Clock (LRCLK)	5	Output	
Bit Clock (BCLK)	11	Output	
SDOUT1	8	Output	
SDOUT2	13	Output	
SDOUT3	3	Output	
SDOUT4	9	Output	
GND	2, 4, 6, 7, 10, 12, 14	Ground	

The nominal signal level is equal to 3.3V. Maximum input level on Master Clock pin is 3.6V.

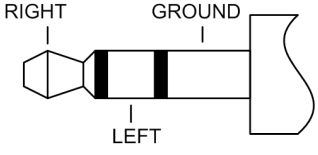
5.5. SPDIF IN / OUT Jack

The SPDIF IN/OUT connector is a 3,5mm audio jack receptacle. The SPDIF signals are also present on standard RCA phono connectors (White->In, Red->Out).

Signal Name	Pin Number	Function	
SPDIF INPUT	Tip	Input	
SPDIF OUTPUT	Ring	Output	
GND	Sleeve	Ground	

5.6. Analogue Output Jack

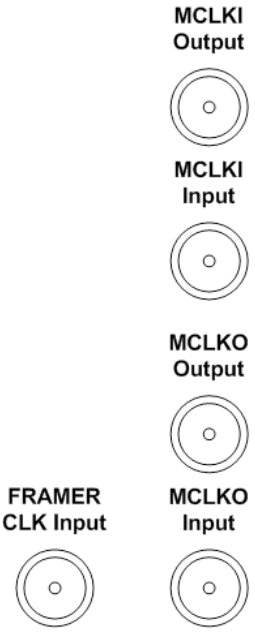
The analogue connector is a 3,5mm audio jack receptacle. The analogue signals are also available on on standard RCA phono connectors.

Signal Name	Pin Number	Function	
Right (DSI stream B)	Tip	Input	
Left (DSI stream A)	Ring	Output	
GND	Sleeve	Ground	

Do not connect loads lower than 300 Ohms.

5.7. Clock Input and Output on SMA connectors

There are five SMA connectors at the top of the case, on the right side. They are al dedicated to clock inputs or clock outputs.



The MCLKI clock input is one of the three clock source for the DSI input interface.

The MCLKI clock output is a buffered output of the clock actually used by the DSI input interface.

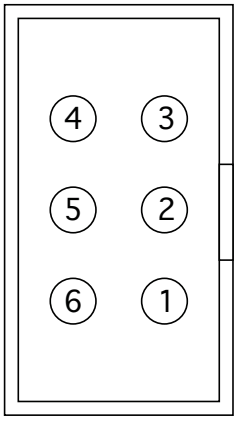
The MCLKO clock input is one of the three clock source for the DSI output interface.

The MCLKO clock output is a buffered output of the clock actually used by the DSI output interface.

The Framer clock input is one of the two clock source for the Framer operation.

All inputs are 100 Ohms terminated. The voltage level at the 100 Ohms load must be comprised between 2V5 and 3V6.

5.8. SLIMbus connector



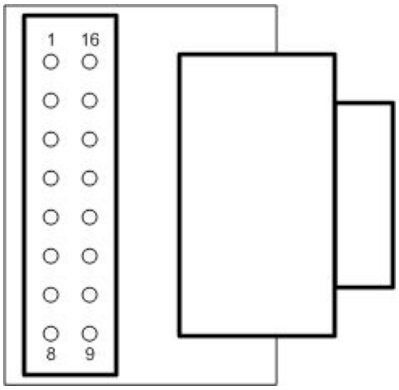
The SLIMbus connector is a DIL6 male pin header (pitch spacing 2,54mm / 0,1”). It is located at the top of the case, in the lower left corner.
The pin assignment is as follow:
1 - SLIMbus Clock
2 - SLIMbus Data
3 - 3V3 power supply (do not connect if not needed)
4 - GND (supply ground)
5 - GND (supply ground)
6 - GND (supply ground)

5.9. DSI adapters

Easy connection to Audio Precision APx analyzer family with DSIO option is provided through a pair of HD15 Male-Female cables. Each end of the cable is a DSI adapter. The 2 adapters are linked by a flat ribbon cable. The user has the possibility to optimize the overall cable length by easily building its own ribbon cable.

Such cable offers good grounding and low capacitive load, making it suitable for high clock frequencies.

5.9.1. DSI IN and DSI OUT adapters

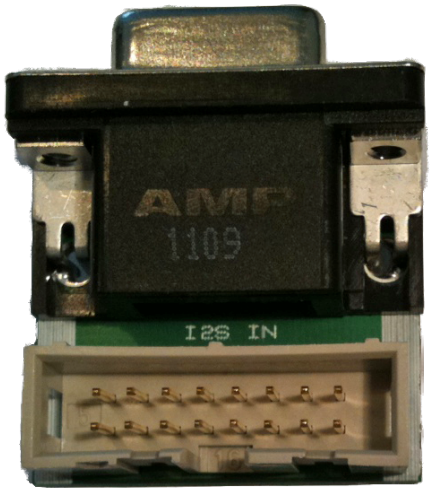


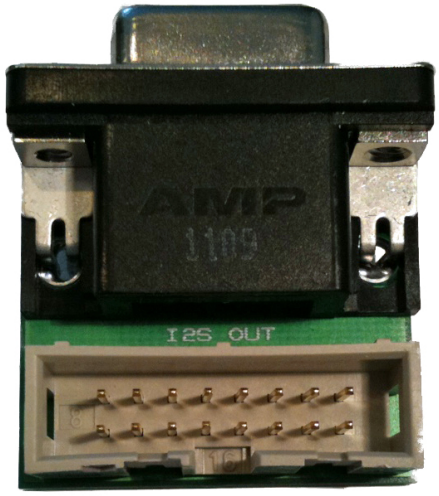
The pin assignment is as follow:

1 - BCLKI (Bit clock at 64Fs)
2 - MCLKI (Master clock at 128Fs or 256Fs)
3 - GND
4 - SDATA1 (Serial data stream 1, 64 bits)
5 - SDATA2 (Serial data stream 2, 64 bits)
6 - SDATA3 (Serial data stream 3, 64 bits)
7 - SDATA4 (Serial data stream 4, 64 bits)
8 - LRCLKI (Word or Sync clock at 1Fs)
9..16 - GND

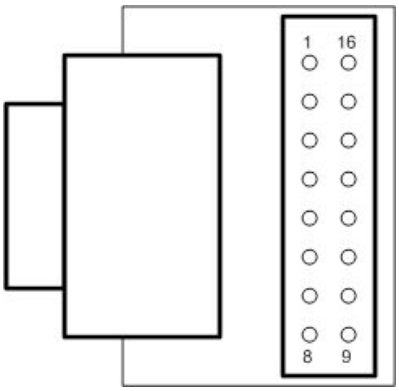
Both DSI IN and DSI OUT adapters have a HD15 female connector. Note that the DSI IN adapter is **NOT** the same as the DSI OUT adapter. Do not interchange them.

The DSI IN adapter has 2 white stripes on each side of the DIL connector and an “I2S IN” print between the HD15 and the DIL connector.
The DSI OUT adapter does not have any white stripes besides the DIL connector and has an “I2S OUT” print between the HD15 and the DIL connector.





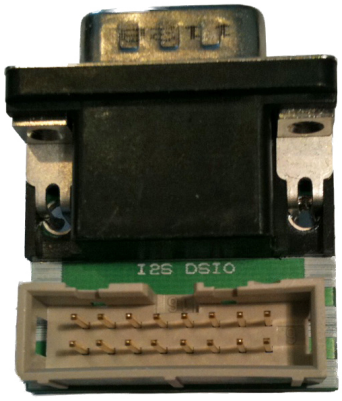
5.9.2. DSIO adapter



The pin assignment is as follow:

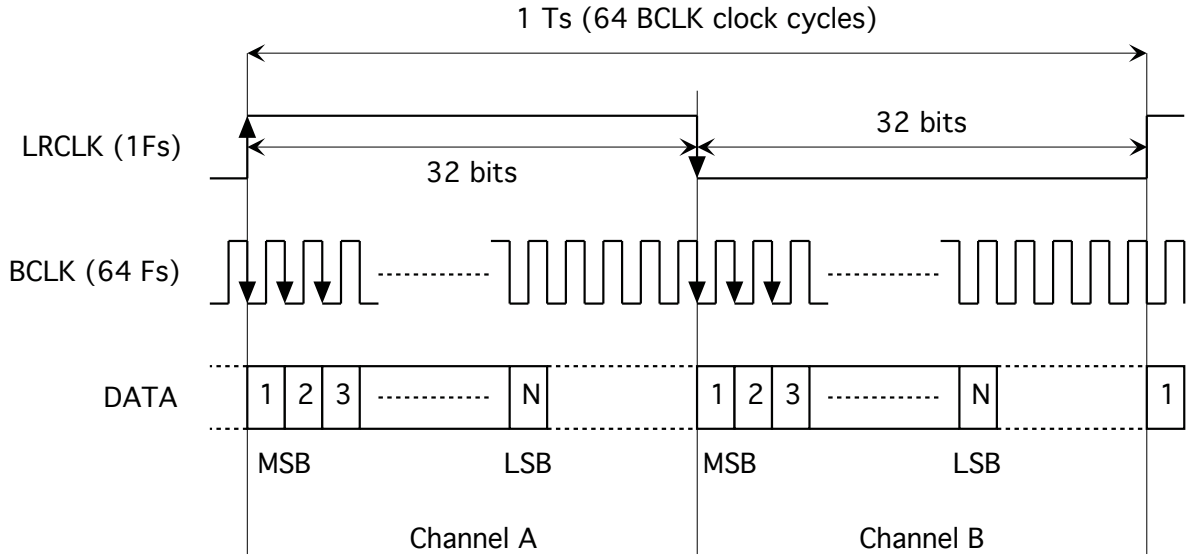
1 - BCLKI (Bit clock at 64Fs)
2 - MCLKI (Master clock at 128Fs or 256Fs)
3 - GND
4 - SDATA1 (Serial data stream 1, 64 bits)
5 - SDATA2 (Serial data stream 2, 64 bits)
6 - SDATA3 (Serial data stream 3, 64 bits)
7 - SDATA4 (Serial data stream 4, 64 bits)
8 - LRCLKI (Word or Sync clock at 1Fs)
9..16 - GND

The DSIO adapter has a male HD15 connector, punctured white stripes on each side of the DIL connector and an “I2S DSIO” print between the HD15 and the DIL connector.



5.10. DSI Data Format

The data are left justified, MSB first and coded on 16 to 24 bits. Data bit set on BCLK falling edge.



6. SLIMbus Operations

The bridge will operate accordingly to the SLIMbus specification.

6.1. Device Enumeration

After the boot sequence, the bridge will send 3 REPORT_PRESENT messages. The Instance Value (IV) of the Enumeration Address depends on the value given to the Component address.

Component address = 0

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0001	0x00	0x00	**0x01C100010000**
Framer	0x01C1	0x0001	0x01	0x00	**0x01C100010100**
Generic	0x01C1	0x0001	0x02	0x00	**0x01C100010200**

Component address = 1

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0001	0x00	0x01	**0x01C100010001**
Framer	0x01C1	0x0001	0x01	0x01	**0x01C100010101**
Generic	0x01C1	0x0001	0x02	0x01	**0x01C100010201**

6.2. Channel Setup

When using the PLLs to generate the audio clocks, some care must be taken to ensure optimal data transmission and / or reception.

The PLLs are configured once the associated Presence Rate is known. The SLIMbus IP communicates that information to the controller when a port is configured and when the associated channel structure and content have been defined by a valid reconfiguration sequence. Note that the channel does not need to be active yet to get the bridge to configure itself for the audio operation.

Once the PLL are configured and stable (it takes less than 3 ms), the channel can be activated and the data streaming will start without any latency or loss of data.

The sequence of message will be as follow:

*** CONNECT_SOURCE or CONNECT_SINK messages ***
BEGIN_RECONFIGURATION
NEXT_DEFINE_CHANNEL(...)
NEXT_DEFINE_CONTENT(...)
RECONFIGURE_NOW
... <--- At that moment, the PLLs get configured
*** Delay for 3 ms ***
...

BEGIN_RECONFIGURATION
NEXT_ACTIVATE_CHANNEL(...)
RECONFIGURE_NOW
... <--- The data streaming is effectively starting

If the channel activation message, there will be a delay of about 3 ms during which the data will either not be transmitted on the bus or not read. When dealing with audio tests, it is definitively not an issue. When it is about verifying that every sample sent is well received, special care must be taken.

Deactivating a channel does not reset the PLL settings. Therefore, the channel can be reactivated at any time and be immediately operational. Only a port reset will affect the PLL configuration.

Note that these recommendations will not apply when an external clock source is used, as the audio clocks are required to be present and stable before the audio channel is activated.

6.3. ASRC Configuration

The bridge uses the DL field (Data Length) to adequately set the output word length of the asynchronous sample rate converter. Dithering is applied on the LSB of the sample for optimal THD+N performances. The data lengths of interest are 16 bits (4 slots), 20 bits (5 slots) and 24 bits (6 slots).

If the DL field is smaller than 4 slots, the ASRC output word length will be set by default to 16 bits. If the DL field is greater than 6 slots or set to “Not Indicated”, the output word length will be set by default to 24 bits. The sample size is displayed on the main page:

```
DSI >ASRC16>SB>SDO2
DSI >ASRC20>SB>SDO2
DSI >ASRC24>SB>SDO2
```

The data length is specified by the Data Length field value in the NEXT_DEFINE_CONTENT message. Make sure that the data Segment is large enough to fit the sample as defined by the DL field. Otherwise, the dithered bit will be lost and the sample truncation will lead to undesired distortions.

If the ASRC is not activated, the DL field value will not have any effect on the bridge.

6.4. Audio Data Format

The bridge supports 2 audio data formats:
- 0 (“Not Indicated”) forces the bridge to use the 2’s complement format of the DSI interface. Note that the DSI format must be **Left Justified, MSB first**.
- 1 (“LPCM”) forces the bridge to use the sign&offset magnitude format defined by the SLIMbus specification. It will convert 2’s complement samples to LPCM and vice&versa.

The data format is specified by the Data Type field value in the NEXT_DEFINE_CONTENT message.

6.5. Using the Value Elements

Most of the bridge parameters can be modified by using the Value Elements of the Generic device. To validate the bits set in the Value Element, the MSB of the Value Element must be set. Otherwise the Value Element content will not have any other effect than being displayed in the page 6 (see section 2.1.7).

The bit assignment is shown in the following table.

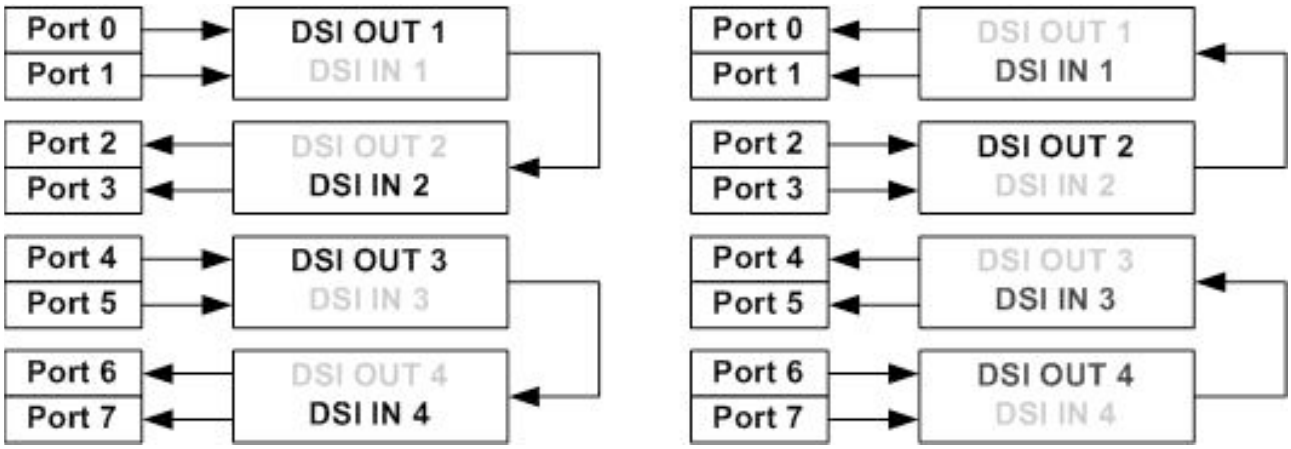
Value Element	Bit	Name	Description
0	0	FRAMER_ENA	Set the bridge Framer as Primary (1) or Inactive (0)
	1	FRAMER_CLK_SEL	Framer clock source: PLL (0) or external (1)
	2	BOOT_RF0	Root Frequency reported by the bridge Framer in the Framing Information at boot time. BOOT_RF[3:0] must use the coding or the RF field as described in the SLIMbus specification. 0b0000➔Not Indicated,0b0001➔24.576MHz, 0b0010➔22,5792MHz, 0b0011➔15,36MHz, 0b0100➔16,8MHz, 0b0101➔19,2MHz, 0b0110➔24MHz, 0b0111➔25MHz, 0b1000➔26MHz, 0b1001➔27MHz
	3	BOOT_RF1	
	4	BOOT_RF2	
	5	BOOT_RF3	
	6	RESET_BRIDGE	Force a bridge reset when set to 1
	7	VE0_VALIDATE	Activate the functions of bit 0 to 6 when set to 1
1	0	MCLKI_SEL0	Set the DSI input master clock mux. 0b00➔PLL, 0b01➔DSI, 0b10➔SMA, 0b11➔Reserved
	1	MCLKI_SEL1	
	2	MCLKO_SEL0	Set the DSI output master clock mux. 0b00➔PLL, 0b01➔DSI, 0b10➔SMA, 0b11➔Reserved
	3	MCLKO_SEL1	
	4	SPDIF_ASRC_ENA	SPDIF Asynchronous Sample Rate status. Enabled when 1
	5	DSI_ASRC_ENA	DSI Asynchronous Sample Rate status. Enabled when 1
	6	BUS_HOLD_ENA	SLIMbus Bus Hold status. Enabled when 1
	7	VE1_VALIDATE	Activate the functions of bit 0 to 6 when set to 1
2	0	LOOPBACK_ENA	Data loop back functionality. Enabled when 1
	1	DAC_SD_SEL0	DAC and SPDIF output data stream selector. 0b00➔SDOUT1, 0b01➔SDOUT2, 0b10➔SDOUT3, 0b11➔SDOUT4.
	2	DAC_SD_SEL1	
	3	DAC_ATTN0	Analogue output level attenuation by steps of 2 dB. It ranges from 0dB (0b0000) to -30 dB (0b1111).
	4	DAC_ATTN1	
	5	DAC_ATTN2	
	6	DAC_ATTN3	
	7	VE2_VALIDATE	Activate the functions of bit 0 to 6 when set to 1

6.6. Loop back mode

The loopback mode is enabled by setting bit 0 of the Value Element 2 (VE2).
When the loopback mode is enabled, the bridge will automatically feed the DSI INPUT interface with the content of the DSI OUTPUT interface.

The 8 Ports bridge has the following internal routing:

- The DSI Output stream 1 (coming from sink Port 0 and 1) is routed to the DSI Input stream 2 (going to source Port 2 and 3).
- The DSI Output stream 2 (coming from sink Port 2 and 3) is routed to the DSI Input stream 1 (going to source Port 0 and 1).
- The DSI Output stream 3 (coming from sink Port 4 and 5) is routed to the DSI Input stream 4 (going to source Port 6 and 7).
- The DSI Output stream 4 (coming from sink Port 6 and 7) is routed to the DSI Input stream 3 (going to source Port 4 and 6).



The 2 ports bridge cannot execute a loop back as only the DSI IN1 and DSI OUT1 are available.

7. Bridge Specifications

Power Supply

Parameter	Min	Typical	Max	Unit
Power supply voltage	7		12	V
Power supply current consumption			0,4	A

HD15 DSI Input Interface

Parameter	Min	Typical	Max	Unit
DSI IN signaling voltage	2,5	3,3	3,6	V
Input pin capacitive load			15	pF
Master clock frequency	1		24,576	MHz
Word clock frequency	4		192	kHz
Bit clock frequency	0,256		12,288	MHz

HD15 DSI Output Interface

Parameter	Min	Typical	Max	Unit
DSI OUT signaling voltage (output)		3,3		V
DSI OUT signaling voltage (input)	2,5	3,3	3,6	V
Input pin capacitive load			15	pF
Master clock frequency	1		24,576	MHz
Word clock frequency	4		192	kHz
Bit clock frequency	0,256		12,288	MHz

SPDIF IN /OUT Interface

Parameter	Min	Typical	Max	Unit
SPDIF IN signaling voltage		1		Vpp
SPDIF IN impedance		75		Ohms
SPDIF OUT signaling voltage		1		Vpp
SPDIF OUT impedance		75		Ohms
Sample Rate (input and output)	32		192	kHz

MCLKI Input (SMA)

Parameter	Min	Typical	Max	Unit
Signaling voltage (source impedance = 0 Ohms)	2,5	3,3	3,6	V
Signaling voltage (source impedance = 50 Ohms)	4,5	5	5,5	V
Input impedance		100		Ohms
Frequency			25	MHz

MCLKI Output (SMA)

Parameter	Min	Typical	Max	Unit
Signaling voltage		3,3		V
Output impedance		50		Ohms
Frequency			25	MHz

MCLKO Input (SMA)

Parameter	Min	Typical	Max	Unit
Signaling voltage (source impedance = 0 Ohms)	2,5	3,3	3,6	V
Signaling voltage (source impedance = 50 Ohms)	4,5	5	5,5	V
Input impedance		100		Ohms
Frequency			25	MHz

MCLKO Output (SMA)

Parameter	Min	Typical	Max	Unit
Signaling voltage		3,3		V
Output impedance		50		Ohms
Frequency			25	MHz

FRAMER Clock Input (SMA)

Parameter	Min	Typical	Max	Unit
Signaling voltage (source impedance = 0 Ohms)	2,5	3,3	3,6	V
Signaling voltage (source impedance = 50 Ohms)	4,5	5	5,5	V
Input impedance		100		Ohms
Frequency			28	MHz

Analogue Output

Parameter	Min	Typical	Max	Unit
Full scale output level		4		Vpp
Output impedance			0,1	Ohms
Bandwidth (-3dB)	3,8		0,546xFs	Hz
Frequency Response Flatness			0,1	dB
THD+N (full scale, 20kHz BW)			0,005	%
Dynamic Range		104		dB

SPDIF ASRC performances

Parameter	Min	Typical	Max	Unit
THD+N (0dBFs, 24 bits resolution)			-140	dB
Dynamic Range		142		dB
Input / Output Sampling Ratio	1:16		16:1	

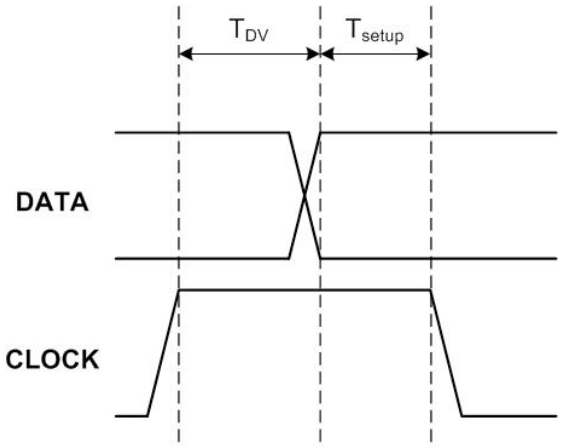
DSI ASRC performances

Parameter	Min	Typical	Max	Unit
THD+N (0dBFs, 24 bits resolution)			-125	dB
Dynamic Range		128		dB
Input / Output Sampling Ratio	1:16		16:1	

SLIMbus Electrical Performances

Parameter	Min	Typical	Max	Unit
Clock Gear range	1		10	
Operating frequency			28	MHz
Signaling voltage	1,2		1,8	V
Bus Hold impedance		33		kOhms
Clock and Data output impedance		22		Ohms
Clock and Data input capacitive load			20	pF

SLIMbus Timing specifications



With Internal Framer:

T_{DV} > 2 ns

T_{DV} < 9.2 ns

With External Framer:

T_{DV} < 17.4 ns

Due to the T_{DV} of the bridge running on external framer and the T_{setup} of the SLIMbus Protocol Analyzer+Traffic Generator, the 2 units can be reliably used together till 20 MHz. Above this frequency, the T_{setup} of the analyzer is violated and the captured results may be corrupted.

Annex A - Presence Rate Compatibility Tables

These tables only apply when **both** input and output master clocks are derived from the PLLs. Green cells indicate a valid combination of input and output presence rates. The value in the cell defines the lowest gear that can be used for the selected presence rates.

Root Frequency 1: 24,576 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	6					6					6					
96		6	6	6	6		6	6	6	6		6	6	6	6	6
48		6	6	6	6		6	6	6	6		6	6	6	6	6
24		6	6	6	6		6	6	6	6		6	6	6	6	6
12		6	6	6	6		6	6	6	6		6	6	6	6	6
176,4	6					6					6					
88,2		6	6	6	6		6	6	6	6		6	6	6	6	6
44,1		6	6	6	6		6	6	6	6		6	6	6	6	6
22,05		6	6	6	6		6	6	6	6		6	6	6	6	6
11,025		6	6	6	6		6	6	6	6		6	6	6	6	6
128	6					6					6					
64		6	6	6	6		6	6	6	6		6	6	6	6	6
32		6	6	6	6		6	6	6	6		6	6	6	6	6
16		6	6	6	6		6	6	6	6		6	6	6	6	6
8		6	6	6	6		6	6	6	6		6	6	6	6	6
4		6	6	6	6		6	6	6	6		6	6	6	6	6

Root Frequency 2: 22,5792 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	8					8/6					8/6					
96		8	8	8	8		8/6	8/6	8/6	8/6		8/6	8/6	8/6	8/6	8/6
48		8	8	8	8		8/6	8/6	8/6	8/6		8/6	8/6	8/6	8/6	8/6
24		8	8	8	8		8/6	8/6	8/6	8/6		8/6	8/6	8/6	8/6	8/6
12		8	8	8	8		8/6	8/6	8/6	8/6		8/6	8/6	8/6	8/6	8/6
176,4	6/8					6					6					
88,2		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
44,1		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
22,05		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
11,025		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
128	6/8					6					6					
64		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
32		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
16		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
8		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6
4		6/8	6/8	6/8	6/8		6	6	6	6		6	6	6	6	6

Root Frequency 3: 15,36 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	7					7					7					
96		7	7	7	7		7	7	7	7		7	7	7	7	7
48		7	7	7	7		7	7	7	7		7	7	7	7	7
24		7	7	7	7		7	7	7	7		7	7	7	7	7
12		7	7	7	7		7	7	7	7		7	7	7	7	7
176,4	7					7					7					
88,2		7	7	7	7		7	7	7	7		7	7	7	7	7
44,1		7	7	7	7		7	7	7	7		7	7	7	7	7
22,05		7	7	7	7		7	7	7	7		7	7	7	7	7
11,025		7	7	7	7		7	7	7	7		7	7	7	7	7
128	7					7					7					
64		7	7	7	7		7	7	7	7		7	7	7	7	7
32		7	7	7	7		7	7	7	7		7	7	7	7	7
16		7	7	7	7		7	7	7	7		7	7	7	7	7
8		7	7	7	7		7	7	7	7		7	7	7	7	7
4		7	7	7	7		7	7	7	7		7	7	7	7	7

Root Frequency 4: 16,8 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	9					9					9/7					
96		9	9/7	9/7	9/7		9	9/7	9/7	9/7		9	9/7	9/7	9/7	9/7
48		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
24		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
12		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
176,4	9					9					9/7					
88,2		9	9/7	9/7	9/7		9	9/7	9/7	9/7		9	9/7	9/7	9/7	9/7
44,1		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
22,05		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
11,025		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
128	7/9					7/9					7					
64		9	9/7	9/7	9/7		9	9/7	9/7	9/7		9	9/8	9/7	9/7	9/7
32		8/9	8/7	8/7	8/7		8/9	8/7	8/7	8/7		8/9	8	9/8	9/8	9/8
16		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
8		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7
4		7/9	7	7	7		7/9	7	7	7		7/9	7/8	7	7	7

Root Frequency 5: 19,2 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	7					7/9					7					
96		7	7/6	7/6	7/6		7/9	7/8	7	7/6		7	7/6	7/6	7/6	7/6
48		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6
24		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6
12		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6
176,4	9/7					9					9/7					
88,2		9/7	9/6	9/6	9/6		9	9/8	9/7	9/6		9/7	9/6	9/6	9/6	9/6
44,1		8/7	8/6	8/6	8/6		8/9	8	8/7	8/6		8/7	8/6	8/6	8/6	8/6
22,05		7	7/6	7/6	7/6		7/9	7/8	7	7/6		7	7/6	7/6	7/6	7/6
11,025		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6
128	7					7/9					7					
64		7	7/6	7/6	7/6		7/9	7/8	7	7/6		7	7/6	7/6	7/6	7/6
32		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6
16		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6
8		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6
4		6/7	6	6	6		6/9	6/8	6/7	6		6/7	6	6	6	6

Root Frequency 6: 24 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	9					9/8					9					
96		9	9/8	9/7	9/6		9/8	9/8	9/7	9/7		9	9/8	9/7	9/6	9/6
48		8/9	8	8/7	8/6		8	8	8/7	8/7		8/9	8	8/7	8/6	8/6
24		7/9	7/8	7	7/6		7/8	7/8	7	7		7/9	7/8	7	7/6	7/6
12		6/9	6/8	6/7	6		6/8	6/8	6/7	6/7		6/9	6/8	6/7	6	6
176,4	8/9					8					8/9					
88,2		8/9	8	7/8	8/6		8	8/7	8/7	8/7		8/9	8	8/7	8/6	8/6
44,1		8/9	8	7/8	8/6		7/8	7	7	7		8/9	8	8/7	8/6	8/6
22,05		7/9	8/7	7	7/6		7/8	7	7	7		7/9	7/8	7	7/6	7/6
11,025		7/9	8/7	7	7/6		7/8	7	7	7		7/9	7/8	7	7/6	7/6
128	9					9/8					9					
64		9	9/8	9/7	9/6		9/8	9/8	9/7	9/7		9	9/8	9/7	9/6	9/6
32		8/9	8	8/7	8/6		8	8	8/7	8/7		8/9	8	8/7	8/6	8/6
16		7/9	7/8	7	7/6		7/8	7/8	7	7		7/9	7/8	7	7/6	7/6
8		6/9	6/8	6/7	6		6/8	6/8	6/7	6/7		6/9	6/8	6/7	6	6
4		6/9	6/8	6/7	6		6/8	6/8	6/7	6/7		6/9	6/8	6/7	6	6

Root Frequency 7: 25 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	6					6/8					6/7					
96		6	6	6	6		6/8	6/7	6	6		6/7	6	6	6	6
48		6	6	6	6		6/8	6/7	6	6		6/7	6	6	6	6
24		6	6	6	6		6/8	6/7	6	6		6/7	6	6	6	6
12		6	6	6	6		6/8	6/7	6	6		6/7	6	6	6	6
176,4	8/6					8										
88,2		8/6	8/6	8/6	8/6		8	8/7	8/6	8/6		8/7	8/6	8/6	8/6	8/6
44,1		7/6	7/6	7/6	7/6		7/8	7	7/6	7/6		7	7/6	7/6	7/6	7/6
22,05		6	6	6	6		6/8	6/7	6	6		6/7	6	6	6	6
11,025		6	6	6	6		6/8	6/7	6	6		6/7	6	6	6	6
128	7/6															
64		7/6	7/6	7/6	7/6		7/8	7	7/6	7/6		7	7	7/6	7/6	7/6
32		6	6	6	6		6/8	7/6	6	6		7	7	7/6	7/6	7/6
16		6	6	6	6		6/8	7/6	6	6		6/7	6/7	6	6	6
8		6	6	6	6		6/8	7/6	6	6		6/7	6/7	6	6	6
4		6	6	6	6		6/8	7/6	6	6		6/7	6/7	6	6	6

Root Frequency 8: 26 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	6					8/6					8/6					
96		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
48		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
24		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
12		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
176,4	6/8					8					8					
88,2		8/6	8/6	8/6	8/6		8	8/7	8/6	8/6		8	8/7	8/6	8/6	8/6
44,1		7/6	7/6	7/6	7/6		7/8	7	7/6	7/6		7/8	7	7/6	7/6	7/6
22,05		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
11,025		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
128	6/8					8					8					
64		8/6	8/6	8/6	8/6		8	8/7	8/6	8/6		8	8/7	8/6	8/6	8/6
32		7/6	7/6	7/6	7/6		7/8	7	7/6	7/6		7/8	7	7/6	7/6	7/6
16		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
8		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6
4		6	6	6	6		6/8	6/7	6	6		6/8	6/7	6	6	6

Root Frequency 9: 27 MHz

Sample Rate	192	96	48	24	12	176	88,2	44,1	22,1	11	128	64	32	16	8	4
192	7					7/8					7/6					
96		7	7/6	7/6	7/6		7/8	7	7/6	7/6		7/6	7/6	7/6	7/6	7/6
48		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
24		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
12		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
176,4	8/7					8					8/6					
88,2		8/7	8/6	8/6	8/6		8	8/7	8/6	8/6		8/6	8/6	8/6	8/6	8/6
44,1		7	7/6	7/6	7/6		7/8	7	7/6	7/6		7/6	7/6	7/6	7/6	7/6
22,05		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
11,025		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
128	6/7					6/8					6					
64		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
32		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
16		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
8		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6
4		6/7	6	6	6		6/8	6/7	6	6		6	6	6	6	6

Annex B - PLL Generated DSI Master Clock Accuracy

These tables only apply when input or output audio master clocks are derived from the PLLs. They list the error applying to the Master clock, either 128 Fs or 256Fs. For instance; the master clock error at 25 MHz Root Frequency for a Presence Rate of 96 kHz is equal to -107 Hz, about 0.000435% deviation from ideal.

	Presence Rate / Master Clock (128 Fs or 256 Fs)				
Root Frequency	192 kHz 24,576 MHz	96 kHz 24,576 MHz	48 kHz 12,288 MHz	24 kHz 6,144 MHz	12 kHz 3,072 MHz
24,576	0	0	0	0	0
22,5792	0	0	0	0	0
15,36	0	0	0	0	0
16,8	0	0	0	0	0
19,2	0	0	0	0	0
24	0	0	0	0	0
25	-107	-107	-54	-27	-13
26	190	190	95	48	-20
27	136	136	68	34	17

	Presence Rate / Master Clock (128 Fs or 256 Fs)				
Root Frequency	176,4 kHz 22,5792 MHz	88,2 kHz 22,5792 MHz	44,1 kHz 11,2896 MHz	22,05 kHz 5644,8 MHz	11,025 kHz 2822,4 MHz
24,576	0	0	0	0	0
22,5792	0	0	0	0	0
15,36	0	0	0	0	0
16,8	0	0	0	0	0
19,2	0	0	0	0	0
24	-253	-253	-126	20	-6
25	-149	-149	-74	-93	3
26	-253	-253	-126	-63	-32
27	212	212	-126	53	3

	Presence Rate / Master Clock (128 Fs or 256 Fs)					
Root Frequency	128 kHz 16,384 MHz	64 kHz 16,384 MHz	32 kHz 8,192 MHz	16 kHz 4,096 MHz	8 kHz 2,048 MHz	4 kHz 1,024 MHz
24,576	0	0	0	0	0	0
22,5792	0	0	0	0	0	0
15,36	0	0	0	0	0	0
16,8	375	0	0	0	0	0
19,2	0	0	0	0	0	0
24	0	0	0	0	0	0
25	-71	-71	-36	-18	-9	-4
26	127	127	63	32	3	8
27	91	91	45	23	1	1