



SLIMbus Multilane Audio Bridge User Manual



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1. Presentation of the tool

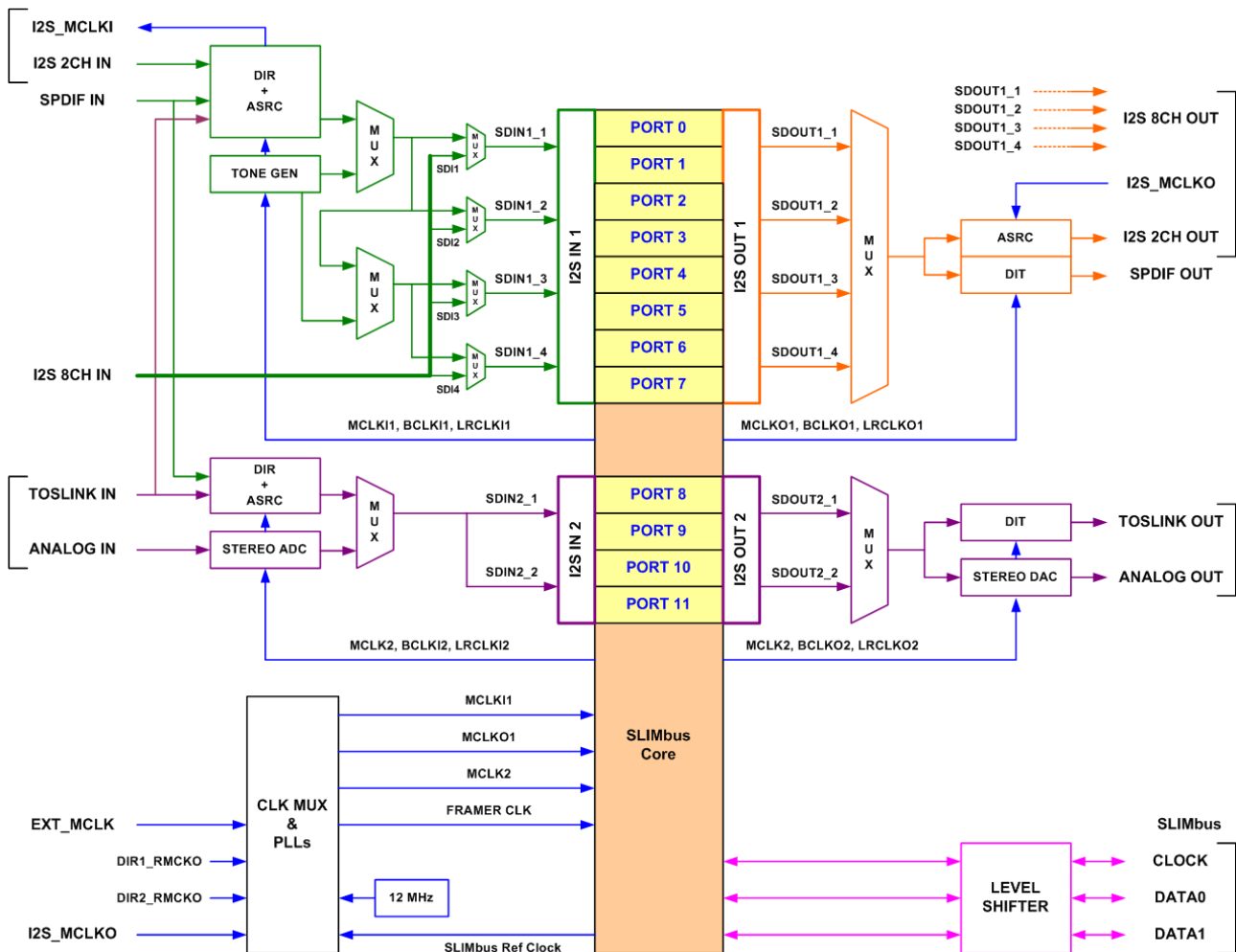
The SLIMbus Multilane Audio Bridge makes the link between SLIMbus Multilane and the analogue and digital legacy audio interfaces.

The main purpose of the bridge is to allow easy tests of audio capabilities of a SLIMbus component with traditional audio analysers (Audio Precision, Rhode&Swartz ...).

The bridge is also a fully featured and compliant SLIMbus component with one Interface device, a Framer device and a Generic device. It can be used to test other SLIMbus components (especially SLIMbus Manager or other audio components).

Main features:

- 12 bidirectional data ports
- 2 SLIMbus data lines
- 3 different and concurrent audio clock domains
- SPDIF input and output
- Optical input and output
- DSI (I2S) stereo input and output
- DSI (I2S) 8 channel input or output (with 4 data lines, no TDM)
- Analogue stereo input and output
- Tone generator (Sine, PRBS & DC value)
- Data loop back function
- Very flexible clock management



SLIMbus Enumeration Address

Component address = 0

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0002	0x00	0x00	0x01C100020000
Framer	0x01C1	0x0002	0x01	0x00	0x01C100020100
Generic	0x01C1	0x0002	0x02	0x00	0x01C100020200

Component address = 1

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0002	0x00	0x01	0x01C100020001
Framer	0x01C1	0x0002	0x01	0x01	0x01C100020101
Generic	0x01C1	0x0002	0x02	0x01	0x01C100020201

Data Port Capabilities

The 12 data ports support the Isochronous, Pushed and Pulled protocols.

The Data Length is up to 32 bits.

Port 0, 1, 8 and 9 are manually configurable to listen to already defined channels.

2. Using the tool

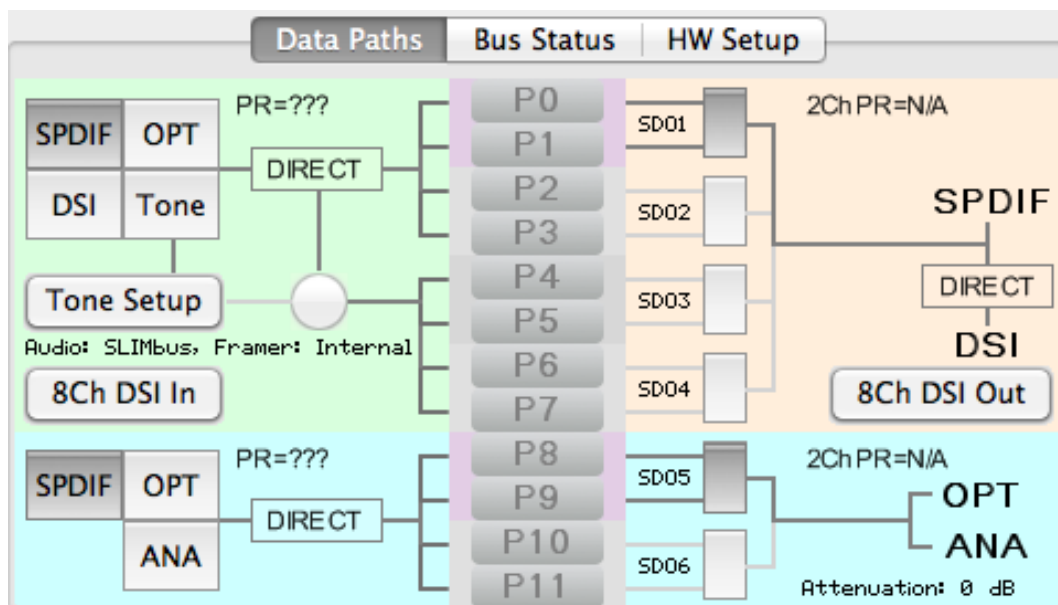
The bridge can operate as a stand alone device. It has its own graphical user interface (4.3" colour display with touch screen) for the required parameter changes.

The GUI is organised in three main pages:

- Data Paths
- Bus Status
- Hardware Setup

2.1. Data Path

This page shows the port status (and associated presence rate), the signal routing and various information like the Sample Rate converter status, the digital receiver status, the loop back configuration...



The Data Ports are numbered from 0 to 11. There are two groups of ports. The first one has the first 8 ports (0 to 7). The second one has the last 4 ports (8 to 11).

The first group uses the clock domain 1 (also referred as MCLKI1) for the Source ports and the clock domain 2 (also referred as MCLKO1) for the Sink ports.

The second group has the same clock domain 3 (also referred as MCLK2) for both Source and Sink ports).

The clock domains are identified by the background colour:

- Clock domain 1 (MCLKI1) : light green
- Clock domain 2 (MCLKO1): light orange
- Clock domain 3 (MCLK2) : light blue

2.1.1. Input Section

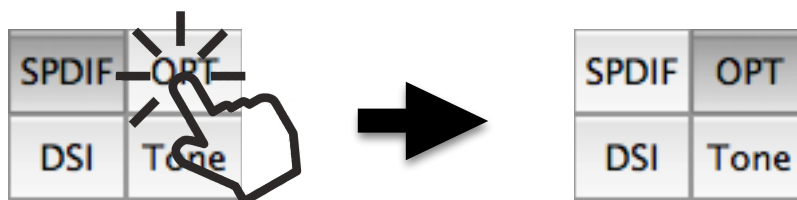
The input signals are shown on the left side of the display. On the clock domain 1, the SPDIF, Optical, DSI stereo and DSI 8 channels inputs are available as well as the internal tone generator. These input signals directly feed the port 0 to 3 inputs. Ports 4 to 7 can be directly fed by the tone generator or by the ports 0 to 3 input signals.

On the clock domain 3, the SPDIF, Optical and analogue inputs are available.

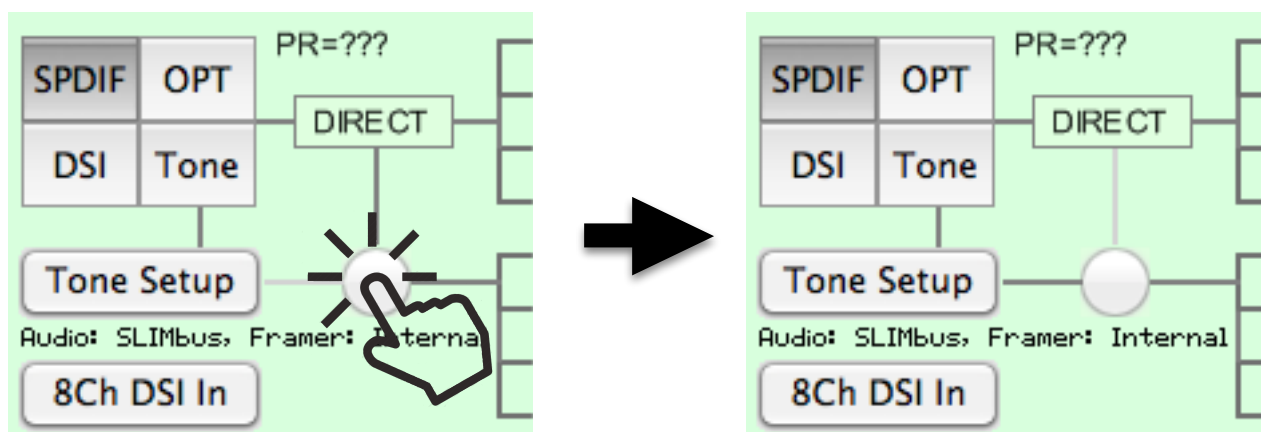
Port Pair	Stream	Input interface	
P0 & P1	SDI1	Stereo SPDIF, Optical, DSI or Tone Generator	DSI 8 Channels
P2 & P3	SDI2		
P4 & P5	SDI3	P0-P3 inputs or Tone Generator	
P6 & P7	SDI4		
P8 & P9	SDI5	Stereo SPDIF, Optical & Analogue	
P10 & P11	SDI6		

An asynchronous sample rate converter (ASRC) is available on each clock domain (1, 2 and 3) in case the signal sampling rate would not match exactly the SLIMbus channel Presence Rate. The ASRC is controlled via the HW Setup pages. When the ASRC is not in use, “**DIRECT**” is shown in the ASRC box. When it is activated, “**ASRCxx**” is shown, where **xx** is the sample size used by the ASRC (it can be 16, 20 or 24 bits).

To Select an input signal, just press the corresponding button.



The input feed of the Ports 4 to 7 is controlled by the round router. Press on it to toggle the data path.



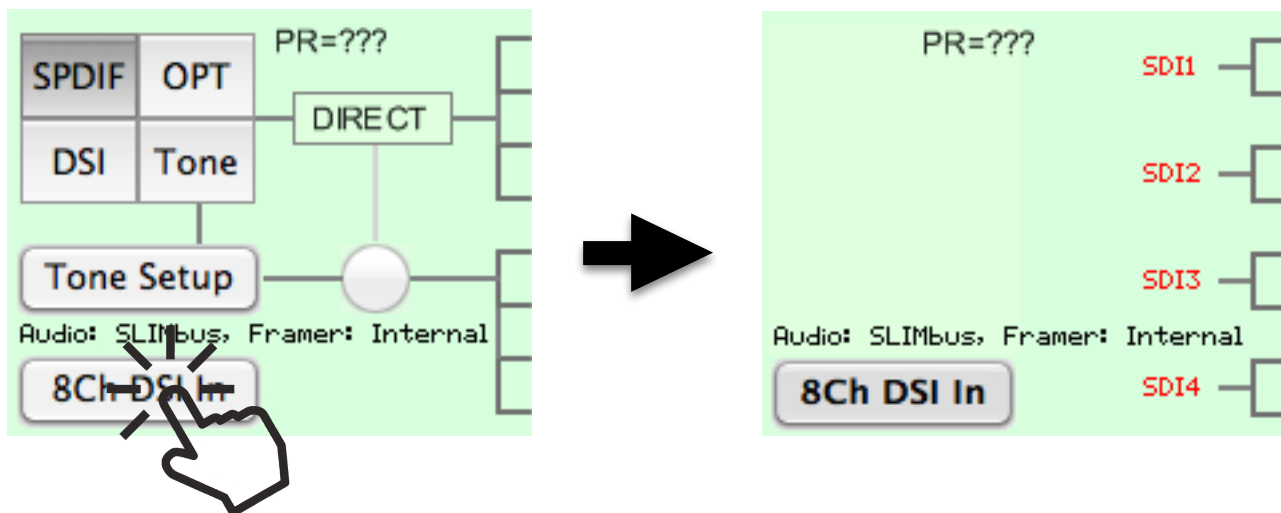
P4-7 inputs = P0-3 inputs

P4-7 inputs = Tone Generator

To activate the 8 channel DSI input, press the button “8Ch DSI In”. In this mode, all the other clock domain 1 inputs are deactivated. The clock domain 2 outputs are also disabled.

The 4 input data streams are fed through the DSI connector. The corresponding word and bit clocks are outputs on the DSI connector (the DSI 8 Ch is always clock master).

Press again the button “8Ch DSI In” to go back to nominal stereo operations.



2.1.2. Tone Generator Setup

To configure the Tone Generator, press the Tone Setup button. A new page will appear with the tone generator parameters.

The Tone Generator has two independent channels. The possible signal types are:

- a constant (DC) value (set by the PC application).
 - a **P**seudo **R**andom **B**it **S**equences (PRBS) based on a 16 bit linear feedback shift register.
 - a selectable waveform (sine, square, triangle) with selectable frequency and amplitude.
- It is also possible to control the delay between the two channels and to sum the two channels on channel A.

The desired output is selected by pressing the corresponding radio button.

The frequency, amplitude and delay are changed by pressing on the text field. A keyboard will appear with a guidance tip. Type the desired value and finish the parameter edition by pressing the validate button.

Ch A Tone Frequency (<Fs/2)

2560

Hz

7	8	9	CANCEL
4	5	6	VALIDATE
1	2	3	
0	.	DEL	CLEAR

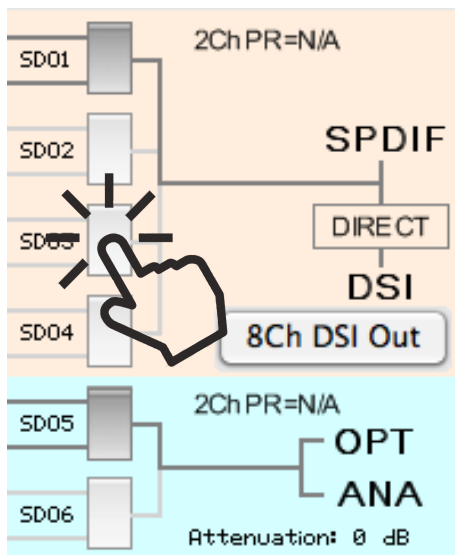
When the Tone Generator parameter edition is finished, press the **Exit** button to go back to the Data Paths page.

2.1.3. Output Section

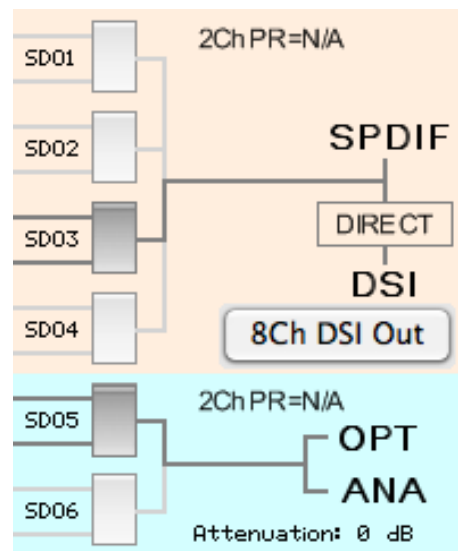
The output interfaces are essentially stereo (two channels). The Data Ports are grouped by pair to output their signals to the selected output interface. As there are more port pairs than available output interfaces, it is necessary to select which port pairs will reach the outputs.

Port Pair	Stream	Output interface	
P0 & P1	SDO1	Stereo SPDIF & DSI	DSI 8 Channels
P2 & P3	SDO2	Stereo SPDIF & DSI	
P4 & P5	SDO3	Stereo SPDIF & DSI	
P6 & P7	SDO4	Stereo SPDIF & DSI	
P8 & P9	SDO5	Stereo Optical & Analogue	
P10 & P11	SDO6	Stereo Optical & Analogue	

The connected stream is selected by pressing the button corresponding to that stream.

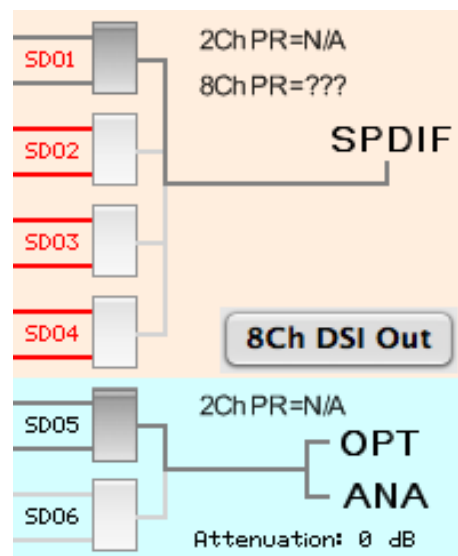
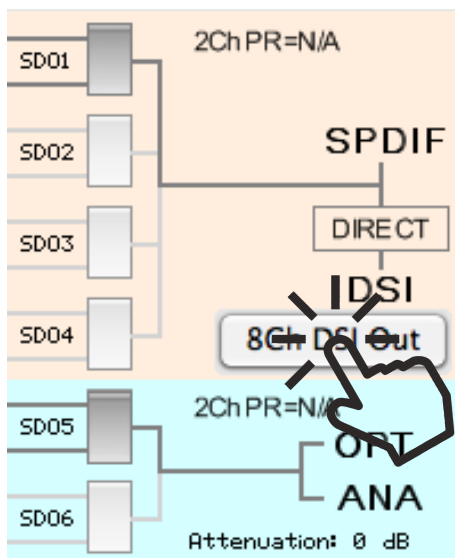


SDO1 on SPDIF & DSI



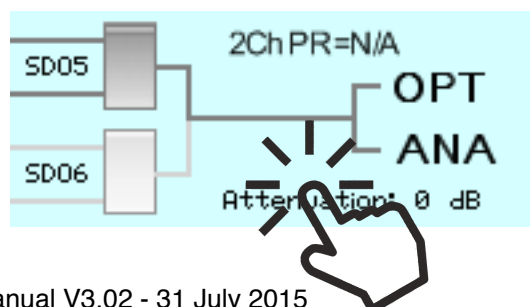
SDO3 on SPDIF and DSI

To activate the 8 channel DSI output, press the “8Ch DSI Out” button.



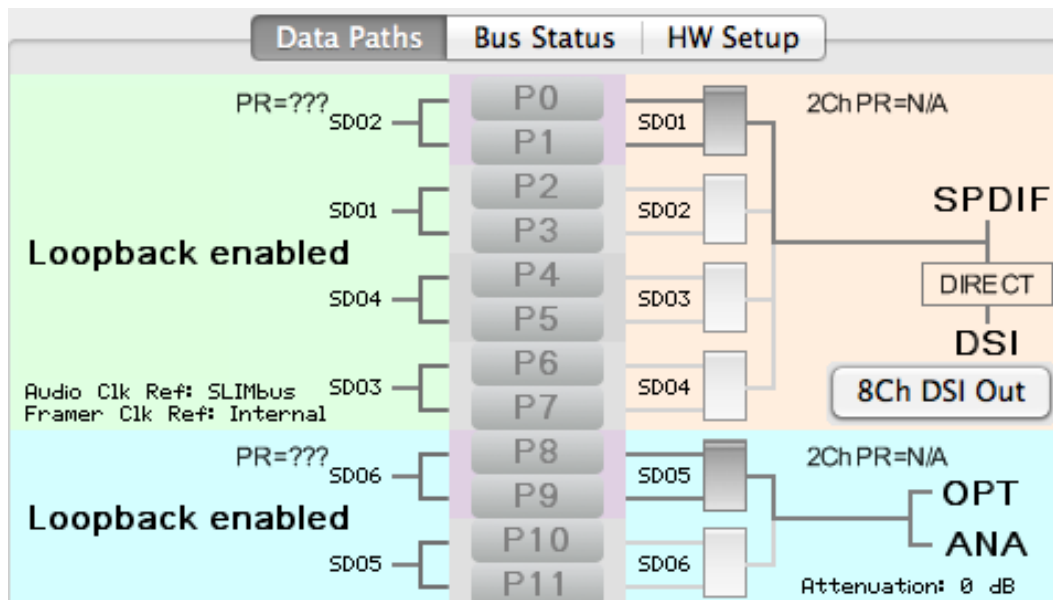
When the 8 channel DSI output is activated, the stereo DSI is disabled. It is still possible to route any of the SDO1 to SDO4 streams to the SPDIF output. In order to operate properly, the 8 channel DSI output requires all the sink ports to use the same presence rate. If it is not the case, the display will show “8Ch PR=Mismatch”.

The analogue output level is controllable. Press anywhere around the text “Attenuation” on the right bottom corner to call the numerical keyboard. Type any value for the attenuation. The value ranges from 0dB to 100 dB by step of 1 dB.



2.1.4. Loopback Mode

The bridge can be placed in loopback mode to re-inject on SLIMbus the data it receives from SLIMbus. The loopback mode is controlled by a Value Element of the Generic device (see section 6.5 of this manual) or directly by the PC application. When the bridge is used in a stand-alone mode, it can only be activated through SLIMbus messages.



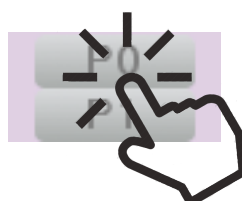
The following table describes the stream connection.

Port Pair	Input Signal
P0 & P1	SDO2
P2 & P3	SDO1
P4 & P5	SDO4
P6 & P7	SDO3
P8 & P9	SDO6
P10 & P11	SDO5

2.1.5. Manual Port Configuration

The Data Ports P0, P1, P8 and P9 can be manually configured to transmit or receive audio streams. The main purpose of that function is to listen to data channel content without having been involved in the channel configuration through SLIMbus messages.

The background behind these port boxes is purple, not grey. Push anywhere in the purple rectangle to call the port configuration panel.



Manual Port Configuration

Port Number: P0, P1, P8, P9

Port Config: Source, Sink, Disconnect

☐ Track Channel # 0

☐ Manual Setup

SD 0 SL 0 TP ISOC PUSHED SD1_ASSIGN

PR 0 DT 1 Line Primary Secondary = 1

Buttons: Exit, Validate

By default, the ports are in the “Disconnected” state. There are two ways to manually configure a data port.

a) Semi-automatic mode

In this mode, the port will track all the messages related to the specified channels. It corresponds to the effect of a CONNECT_ message. The remaining of the port configuration is left to the SLIMbus protocol. To activate that mode, select a port configuration that is either Source or Sink then press the radio button **Track Channel**. Push on the text field to call the keyboard and enter a channel number.

Manual Port Configuration

Port Number: P0, P1, P8, P9

Port Config: Source, Sink, Disconnect

☒ Track Channel # 2

☐ Manual Setup

SD 0 SL 0 TP ISOC PUSHED SD1_ASSIGN

PR 0 DT 1 Line Primary Secondary = 1

Buttons: Exit, Validate

To finish the port configuration, press the **Validate** button. Once the desired ports are configured, press the **Exit** button to go back to the **Data Paths** page.

b) Manual Setup

In this mode, all the data channel parameters must be manually programmed. The full manual configuration corresponds to the complete channel configuration sequence:

- CONNECT_SINK or CONNECT_SOURCE
- BEGIN_RECONFIGURATION
- NEXT_DEFINE_CHANNEL
- NEXT_DEFINE_CONTENT
- NEXT_ACTIVATE_CHANNEL
- RECONFIGURE_NOW

Enter all the parameters by pushing on the text field or pressing the buttons. The parameters take the values as shown in the SLIMbus specification. The keyboard tip guides the user when giving a value to a parameter.

- SD is the Segment Distribution
- PR is the Presence Rate
- SL is the Segment Length
- DT is the Data Type
- TP is the Transport Protocol
- Line is the data line on which the channel appears
- SD1_ASSIGN is the mapping of the bridge data pin 1 to a given data line.

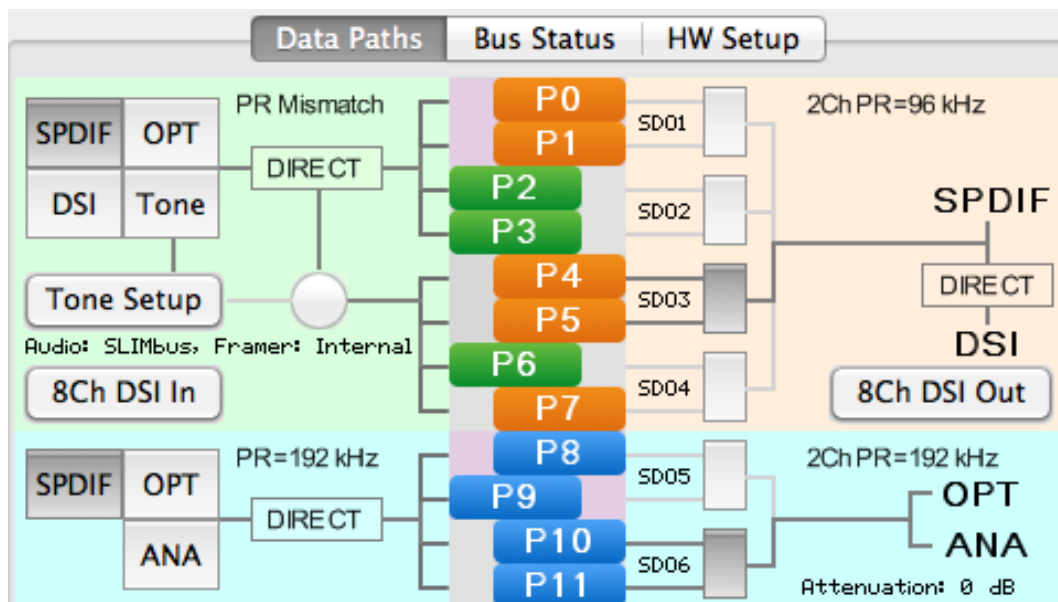
Note: When used as a sink, the port protocol PUSHED correspond to both PUSHED and PULLED, the Presence bit being the same for both protocol. It is important to understand that the manual configuration mode is essentially designed to sniff the content of a data port without disturbing it. Therefore, the manually configured port will not act as an active port with the PULLED protocol.

The image shows a 'Manual Port Configuration' dialog box. At the top, 'Port Number' has buttons for P0, P1 (selected), P8, and P9. Below it, 'Port Config' has buttons for Source, Sink (selected), and Disconnect. There are 'Exit' and 'Validate' buttons on the right. Under 'Track Channel #' is a text field with '0'. Below that, 'Manual Setup' is selected with a radio button. The settings are: SD (3140), SL (6), TP (ISOC, PUSHED), PR (3), DT (1), Line (Primary, Secondary), and SD1_ASSIGN (= 1).

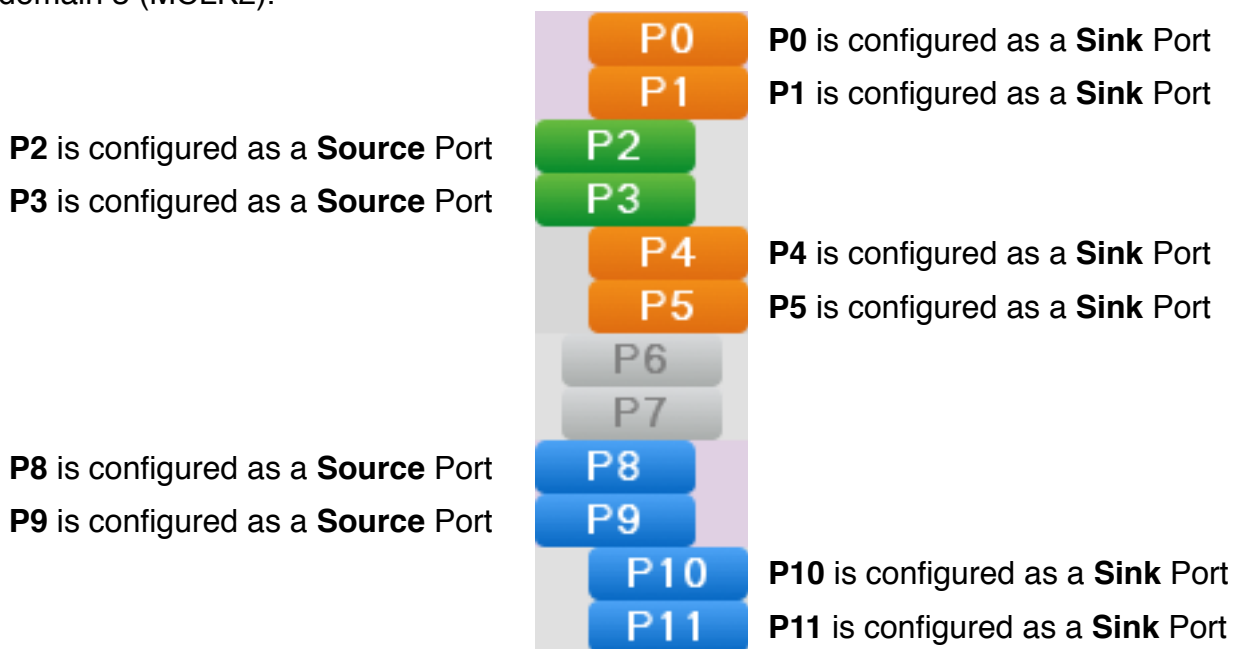
Once a manually configured channel is active, the port text is yellow, not white, to show the user that the port has a special behaviour.

2.1.6. Port Status

When a port is not configured, it appears grey in the middle of the central bar. When a port is fully configured, its position and colour change depending on the function and clock domain to which it belongs.



The source ports 0 to 7 will appear on the left side, coloured in green. The sink ports 0 to 7 will appear in the right side, coloured in orange. The source ports 8 to 11 will appear on the left side, coloured in blue. The sink ports 8 to 11 will appear on the right side, coloured in blue. The source and sink ports are both blue because they belong to the same clock domain 3 (MCLK2).

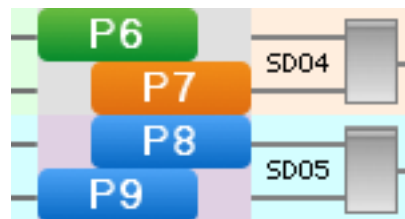


The presence rate is indicated once the ports are configured.

Note: The source ports of each group must use the same Presence Rate because they all use the same audio master clock. The sink port pairs can have different Presence Rate as long as the stereo interfaces are used. The master clock is changed each time a new port pair is selected. When using the 8 channel DSI output mode, all the sink ports of the first group must use the same Presence Rate.

It is possible to configure only one port of a pair or to have the two ports of a pair configured differently. In this case, the digital stereo stream connecting the SLIMbus port to the legacy interface will only carry one audio channel, the other one will carry 0s.

In this example, P6 will transport the channel B of the input stream SDI4. P7 will feed the channel A of the stream SDO4. P8 will feed the channel B of the stream SDO5 and P9 will transport the channel A of the input stream SDI5.



2.2. Bus Status

This page displays the recorded bus configuration and the SLIMBus related registers of the bridge.

The screenshot shows a software interface with three tabs: 'Data Paths', 'Bus Status' (selected), and 'HW Setup'. The 'Bus Status' tab is divided into four sections:

- Framing Information:**
 - Subframe Mode : 19 (4/32)
 - Clock Gear : 9 (6.4->14.4 MHz)
 - Root Frequency : 1 (24.576 MHz)
- Bus Clock:**
 - Programmed Bus Clock : 12.2880 MHz
 - Measured Bus Clock : 0.0000 MHz
 - Internal Framer Status : Inactive
- Physical Layer:**
 - Level : 1.80
 - Bus Hold : ON
 - SD1_ASSIGN : 0
- Bridge VE:**
 - GenDev VE0 : 0
 - GenDev VE1 : 0
 - GenDev VE2 : 0
 - GenDev VE3 : 0
 - GenDev VE4 : 0

The Framing Information is decoded and displayed. The Subframe Mode, Clock Gear and Root Frequency are explicitly shown.

The programmed bus clock and the measured bus clock are shown for comparison. They must match. The framer status indicates if the bridge is the active framer or not.

The physical layer information shows the programmed signaling level, the bus hold status and the data line mapping of the data pin 1 (SD1). This value reflects the content of the Value Element **0x400** of the Interface device.

The five Geberic device Value Elements are also shown. These value elements are used to remote control the bridge (see section 6.5 of this document).

2.3. Hardware Setup

This page has five sub-pages, each dedicated to a specific function of the bridge.

- SLIMbus configuration
- Audio setup
- External clock configuration
- Reference clock selection
- Hardware information and diagnostic

The sub-page navigation relies on the bottom button bar.

2.3.1. SLIMbus Core Configuration

This panel allows the configuration of the various SLIMbus related parameters.

The screenshot shows the 'HW Setup' tab selected. Under 'SLIMbus Configuration', the PHY Signaling Level is 1.80 V, Bus Hold is On, Component Address is 0, and Framer Boot Mode is Primary. Under 'Boot Framing Information', Subframe Mode is 19, Clock Gear is 9, and Root Frequency is 1. A 'Reset SLIMbus Core' button is present. The bottom navigation bar shows 'SLIMbus' as the active section.

The PHY signaling voltage can take any value from 0.9V to 3.2V (3.3V compatible) by step of 50 mV. Press the text field to call the display and type the desired value. The 50mV rounding is handled automatically.

The Bus Hold can be enabled or disabled. If there is a Bus Hold active somewhere on the SLIMbus, the bridge Bus Hold can be disabled. If not, there must be at least one active bus hold to guarantee error free operation and the bridge Bus Hold must be set.

The Component Address (=Instance Value) can take the value 0 or 1. This allows the operation of two bridges on the same SLIMbus.

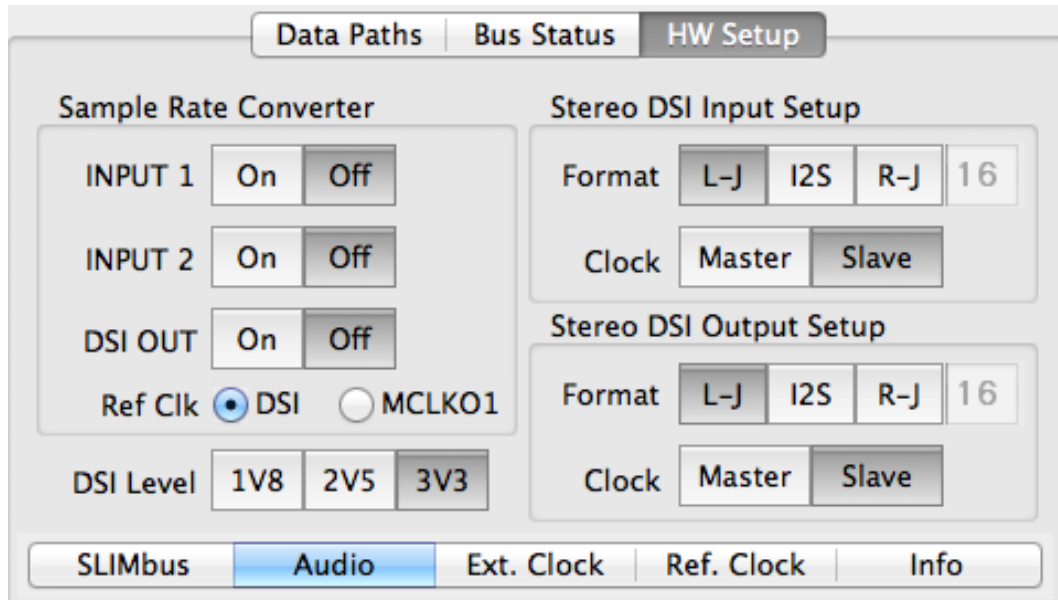
The bridge Framer can be set as the Primary bus framer or not. By default, it should be disabled.

The Boot Framing Information are fully programmable. The framer will use these values when it boot the bus.

Finally, the SLIMbus core can be reset. This function shall be used when the boot mode or the boot framing information are changed and needed to be used immediately. Note that this is a full reset and that the bus will be completely reset also.

2.3.2. Audio Setup

This panel groups all the audio interface parameters that can be programmed.



Asynchronous Sample Rate Converters

There are three sample rate converters in the bridge. Two are located at the inputs and one at the DSI output. They can be turned ON or OFF.

The sample rate converter (ASRC) shall be used (turned ON) when the input sampling rate does not match exactly the SLIMbus channel presence rate. If the ASRC is OFF, samples will be missed or repeated, inducing THD. In the other hand, the use of an ASRC is not benign. It introduces a delay, pre and post ringing in the time domain and measurable ripple in the frequency domain. When a bit perfect transmission is required, the best practice is to clock the audio section of the bridge and the audio source with the same master clock.

The DSI output ASRC can get two reference clocks: the internal MCLKO1 (clock domain 2) or the DSI MCLK input. This is to be used if the receiver connected to the bridge output cannot cope with the sample rate provided by the bridge. By default, this ASRC should be left OFF.

Stereo DSI Interface configuration

The signaling level of the DSI interface is programmable and can be 1.8V, 2.5V or 3.3V.

Both stereo DSI input and output have programmable format and sample size. The format can be Left-Justified, Philips I2S or Right-Justified. When selecting Right-Justified, the sample size must be programmed for proper operation. The sample size can be 16, 20 or 24 bits.

The interfaces can be clock master (active drive of the BCLK and LRCLK) or slave to the BCLK and LRCLK.

2.3.3. External Clock Configuration

This panel groups all the controls related to the external clock management. The bridge has a single SMA connector to either input or output a clock signal. These controls program the behaviour of that connector.

The screenshot shows the 'External Clock Configuration' window. At the top, there are three tabs: 'Data Paths', 'Bus Status', and 'HW Setup'. The 'HW Setup' tab is active. Below it, there are five sub-tabs: 'SLIMbus', 'Audio', 'Ext. Clock' (which is highlighted in blue), 'Ref. Clock', and 'Info'. The 'Ext. Clock' sub-tab contains the following controls:

- Direction:** Two buttons, 'Input' and 'Output'. 'Output' is selected.
- Signaling Level:** Three buttons, '1V8', '2V5', and '3V3'. '1V8' is selected.
- Impedance:** Two buttons, '50R' and '1M'. '50R' is selected.
- Frequency:** A text field showing 'n/a'.
- Output Clock Source:** Two main sections. The 'Framer PLL' section has 'User' and 'Framer' buttons, with 'Framer' selected. Below it is a text field showing '9.600' and 'MHz'. The 'Audio PLL' section has three buttons: 'MCKI1', 'MCKO1', and 'MCK2'. 'MCKO1' is selected.
- Output Clock Divider:** Five buttons: 'None', '/2', '/4', '/?', and '16'. 'None' is selected.
- Frequency:** A text field showing 'n/a'.

The main controls are the clock direction (input or output) and the clock signaling level (1.8V, 2.5V and 3.3V).

Input Clock

When configured as an input, the input impedance can be set to 50Ω or to high impedance (typically >1 MΩ). The SMA connector has a characteristic impedance of 50Ω and can be used to achieve long connection of high frequency signals without suffering reflections.

If the clock source has a 50Ω output impedance, the signaling level at the connector input will be half of the output level of the source. Select the signaling voltage accordingly.

For instance, a source generating a 3.3V clock signal will end up being 1.65V at the bridge SMA connector. Therefore, select 1.8V for optimal operation.

If the clock source is only capable of sourcing 1.8V, it might be wise to shorten the link, to set the input impedance to 1M and to set the signaling voltage to 1.8V.

The bridge constantly measures the frequency of the signal present on the SMA connector and displays it.

Output Clock

When configured as an output, the SMA provides a variety of clock signals. The output impedance is fixed at 50Ω. The output clock source is selectable. It can be a user defined frequency (derived from framer PLL ref clock), the framer reference clock (CG10), the audio MCLKI1, MCLKO1 or MCLK2. The selected frequency can be divided by an integer number to accommodate various use cases. The displayed frequency is measured and is provided to monitor the output.

Not all integer factors are available to divide the clock. It all depends on the PLL settings. If the desired clock is obtain, all is fine. If the measured clock is either 0 or some other unexpected values, then the desired frequency is not reachable.

2.3.4. PLL Reference Clock Selection

Both framer and audio PLLs can be fed by various clocks. This panel is used to select which clock will feed which PLL.

The screenshot shows the 'Internal Clock Configuration' window with the 'HW Setup' tab selected. The window is divided into two main sections: 'Framer PLL clock ref.' and 'Audio PLL clock ref.'. Each section contains a list of clock sources and a frequency display. The 'Framer PLL clock ref.' section shows 'INTERNAL' selected, with frequencies of 0.000 MHz for SPDIF IN, OPTICAL IN, DSI MCLK, and SMA. The 'Audio PLL clock ref.' section shows 'SLIMbus' selected, with frequencies of 0.000 MHz for SPDIF IN, OPTICAL IN, DSI MCLK, and SMA. At the bottom, there are tabs for SLIMbus, Audio, Ext. Clock, Ref. Clock (selected), and Info.

Framer PLL clock ref.		Audio PLL clock ref.	
INTERNAL		SLIMbus	
SPDIF IN	0.000 MHz	SPDIF IN	
OPTICAL IN	0.000 MHz	OPTICAL IN	
DSI MCLK	0.000 MHz	DSI MCLK	
SMA	0.000 MHz	SMA	

SLIMbus Audio Ext. Clock Ref. Clock Info

Framer Reference Clocks

The framer PLL can be fed by several clock sources:

- Internal oscillator: a low jitter 12 MHz clock.
- SPDIF input recovered master clock. Usually at $256 \times F_s$
- Optical input recovered master clock. Usually at $256 \times F_s$
- DSI master clock input.
- External clock input (on SMA).

Note that the reference clock does not need to match the desired framer clock. The bridge measures all the clocks and configures the PLL accordingly. If the selected clock appears to have the same frequency as the targeted clock, the PLL is bypassed.

The four frequencies are measured and displayed to help the user to select the proper clock source.

Framer Reference Clocks

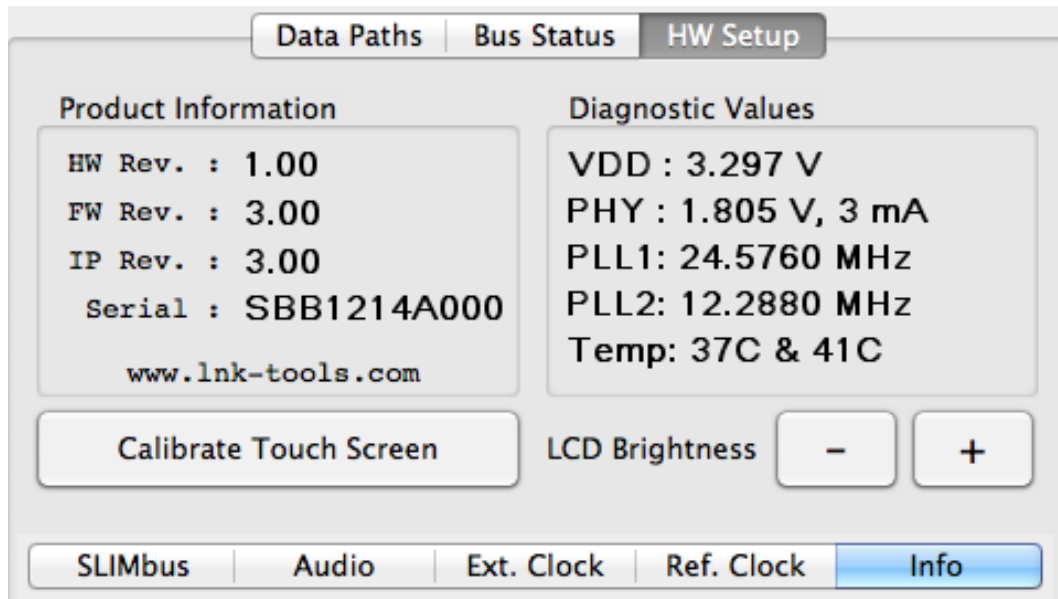
The Audio PLL can be fed by several clock sources:

- SLIMbus clock
- SPDIF input recovered master clock. Usually at $256 \times F_s$
- Optical input recovered master clock. Usually at $256 \times F_s$
- DSI master clock input.
- External clock input (on SMA).

When using the SLIMbus clock, the clock gear shall stay above 5 (CG6 to CG10). Below that frequency (<1.5 MHz), the Audio PLL will not lock properly anymore and the results will not be guaranteed. As for the framer PLL, if the selected clock appears to have the same frequency as the targeted clock, the PLL is bypassed. This property is useful to feed a master clock below 1.5 MHz into the bridge.

2.3.5. Product Information and Diagnostic Values

The panel shows the product information: hardware revision, firmware revision, IP revision and the serial number.



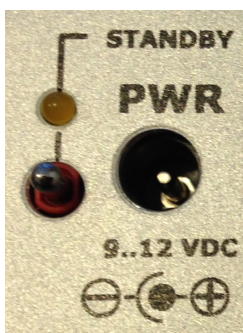
The diagnostic values show the measured main 3.3V supply voltage, the measured SLIMbus PHY voltage and consumed current, the Framer PLL (PLL2) monitoring output, the audio PLL (PLL1) monitoring output and the temperature measured by two internal sensor.

On this panel, it is also possible to dim the LCD backlight. If the unit has to be tuned ON permanently, we strongly recommend to dim the backlight to the minimum. The typical life time of the backlight is 20000 hours, which corresponds to 2.3 years of continuous operation. By dimming the backlight to the minimum, the display life time can be extended to 5 years of continuous operation.

2.4. Standby Switch

The standby switch is located besides the DC barrel jack, on the right side of the hardware. Toggle the switch (up or down) to activate the standby mode.

The display backlight will be switched off, the interfaces will be disconnected and the auxiliary power supplies will be switched off. Sleep modes are activated wherever possible.



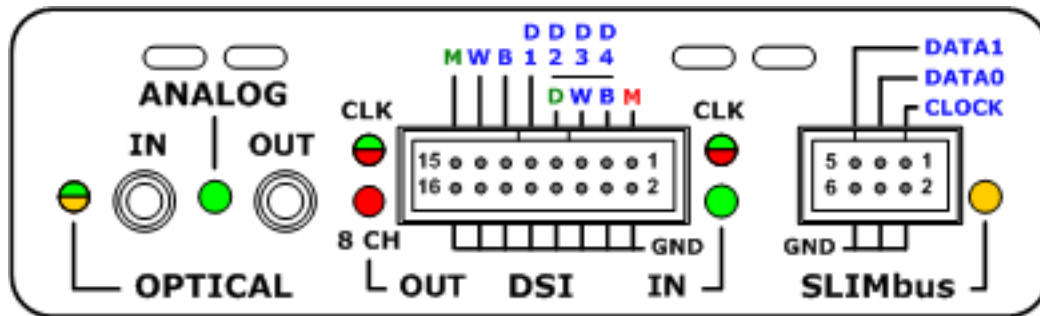
When in standby mode, the yellow led located on top of the standby switch is ON to indicate that the bridge is powered but sleeping.

The bridge will also wake up if it receives a command from its PC application.

Using the standby mode allows the bridge to wake up almost instantaneously (much faster than with a power on).

3. Bridge Connectivity

The bridge interfaces are located on the left and right side of the box. LEDs are often associated to the connectors to indicate a status.



3.1. SLIMbus Connector

PIN	SLIMbus signals	DIR
1	CLOCK	IN / OUT
3	DATA0 (Primary)	IN / OUT
5	DATA1 (Secondary)	IN / OUT
2, 4 & 6	GND	

Type: Standard 6 pin boxed header with pitch of 0.1”.

The yellow led on the left side of the connector is ON when the connector pins are connected to the internal circuitry. It is possible to disable the SLIMbus connector while the bridge is powered by typing 0 in the PHY signalling level text field. When the bridge is in stand-by mode, the SLIMbus connector is also disabled. The SLIMbus IOs operates on a programmable level that ranges from 0.9V to 3.2V

3.2. DSI Connector

PIN	STEREO I2S IN & OUT		DIR	8CH I2S OUT	DIR	8CH I2S IN	DIR
1	DSI IN	MCLKI	OUT	MCLKI	OUT	MCLKI	OUT
3		BCLKI	IN / OUT	SDO4	OUT	SDI4	IN
5		LRCLKI	IN / OUT	SDO3	OUT	SDI3	IN
7		SDIN	IN	SDO2	OUT	SDI2	IN
9	DSI OUT	SDOUT	OUT	SDO1	OUT	SDI1	IN
11		BCLKO	IN / OUT	BCLKO	OUT	BCLKI	OUT
13		LRCLKO	IN / OUT	LRCLKO	OUT	LRCLKI	OUT
15		MCLKO	IN	MCLKO	IN	MCLKO	IN
2..16	GND						

Type: Standard 16 pin boxed header with pitch of 0.1”.

There are four LEDs around the DSI connector.

- The bottom right green LED indicates that the DSI stereo input is used as input.
- The bottom left red LED indicates that the 8 channel DSI output is active.
- The top right bicolour LED indicates whether the DSI stereo output is clock master (red) or clock slave (green).
- The top left bicolour LED indicates whether the DSI stereo input is clock master (red) or clock slave (green).

All the DSI IOs operate on a programmable level that can be 1.8V, 2.5V or 3.3V.

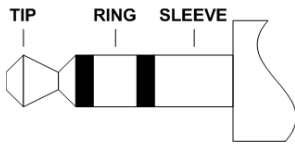
The source impedance of the DSI outputs is equal to **50Ω**.

The input impedance of the DSI inputs is greater than **1MΩ**.

When feeding a clock signal to the MCLKO pin, pay attention to the cable length for reliable operation.

3.3. Optical and Analogue Input Connector

The Optical (TOSLINK) and analogue inputs are sharing the same 3.5mm jack connector. They cannot be used both at the same time.

PIN	Analogue signals	DIR	
TIP	LEFT channel	IN	
RING	RIGHT channel	IN	
SLEEVE	GND		

The bicolour LED on the left side of the input connector indicates that the Optical input is selected and if the receiver detects a valid IEC60958 audio digital stream.

Optical input not selected: all LEDs OFF

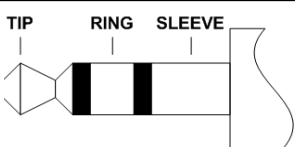
Optical input selected but no valid stream: yellow LED ON

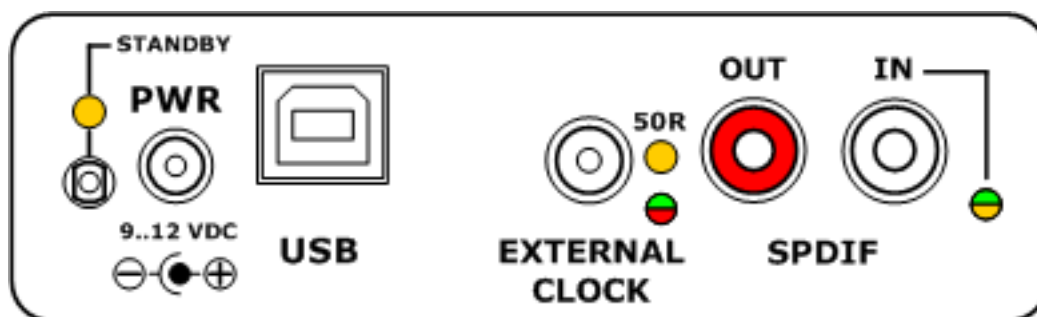
Optical input selected with a valid stream: green LED ON

The green LED on the right side of the input connector indicates that the analogue input is selected.

3.4. Optical and Analogue Output Connector

The Optical (TOSLINK) and analogue outputs are sharing the same 3.5mm jack connector. They cannot be used both at the same time.

PIN	Analogue signals	DIR	
TIP	LEFT channel	OUT	
RING	RIGHT channel	OUT	
SLEEVE	GND		



3.5. SPDIF Input Connector

The SPDIF connector is a standard RCA (cinch) connector. The input impedance is **75Ω**.

The bicolour LED on the right side of the input connector indicates that the SPDIF input is selected and if the receiver detects a valid IEC60958 audio digital stream.

SPDIF input not selected: all LEDs OFF

SPDIF input selected but no valid stream: yellow LED ON

SPDIF input selected with a valid stream: green LED ON

3.6. SPDIF Output Connector

The SPDIF connector is a standard RCA (cinch) connector. The output impedance is **75Ω**.

3.7. External Clock Connector

The external clock connector is a female SMA RF connector. Its characteristics impedance is **50Ω**. The input impedance is switchable between **50Ω** and **1MΩ**.

The bicolour LED at the bottom right side of the SMA connector indicates the direction of the signal. Green, it is set as an input. Red, it is set as an output.

When the yellow LED at the top right of the SMA connector is ON, the **50Ω** input impedance is active.

3.8. USB 2.0 Connector

The USB 2 connector is used to remote control the bridge from a PC. The bridge is self powered and does not consume any power from the USB. Refer to the Audio Bridge software user manual for more detailed information.

3.9. DC Supply Barrel Jack

This is the power supply connector of the bridge. The positive voltage is applied to the centre pin.

Pin	Signal	DIR	
Centre pin	VCC (9V to 12V)	IN	
Outer ring	GND		

3.10. DSI cable adapters

Easy connection to Audio Precision APx analyser family with DSIO option is provided through a pair of custom cables. The cables are made of standard flat cables (16 ways) and standard plugs. The user can easily build its on length of cable but be aware of the propagation delays (about 1ns per15cm of cable).

DSI 8 Channel Output Cable

The cable has a pin header socket on one side (to connect to the bridge DSI) and a APx DSIO Receiver adapter on the other side. This cable shall only be used to transport the 8 channels from the bridge to the APx.

To DSIO Receiver or Transmitter



DSI Stereo Input and Output Cable

The cable has a pin header socket on one side (to connect to the bridge DSI) and a pair of APx DSIO Receiver **AND** Transmitter adapters. This cable shall only be used when stereo connections are required from and to the APx analyser. The adapters have markings to help identifying the DSIO connector it shall connect to.

To DSIO Transmitter



To DSIO Receiver

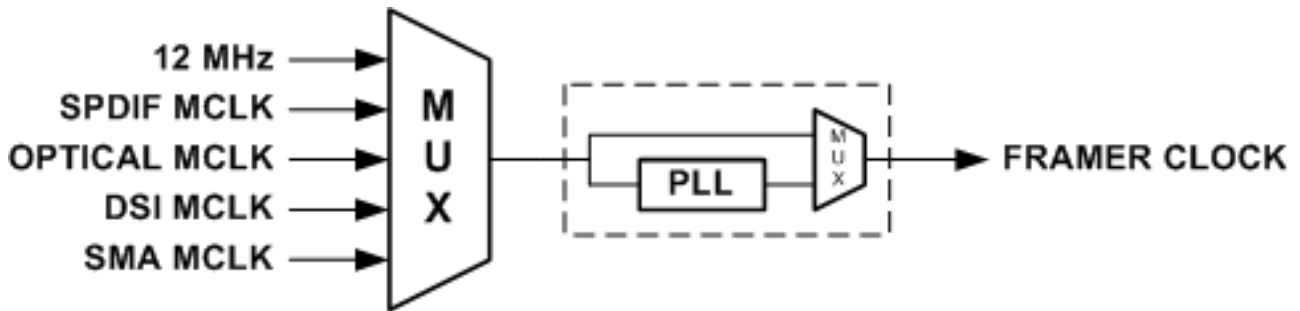
Refer to the Audio Precision DSIO module documentation for detailed information on the DSIO connector pinning.

4. Clock Management

The bridge has a powerful and flexible clock management scheme.

4.1. Framer Clock Generation

The Framer reference clock corresponds to the Root Frequency to be used on SLIMbus. If RF1(24.576MHz) has to be used, the framer clock generator will feed the SLIMbus Core with a frequency equal to 24.576 MHz.



The framer clock can be generated by using five input clocks. The default one is the internal 12 MHz clock source. If the bridge framer must be frequency locked to another clock domain, any of the four other inputs can be used. The most accurate results will be obtained from the DSI master clock input (on pin 15) or from the external clock SMA connector.

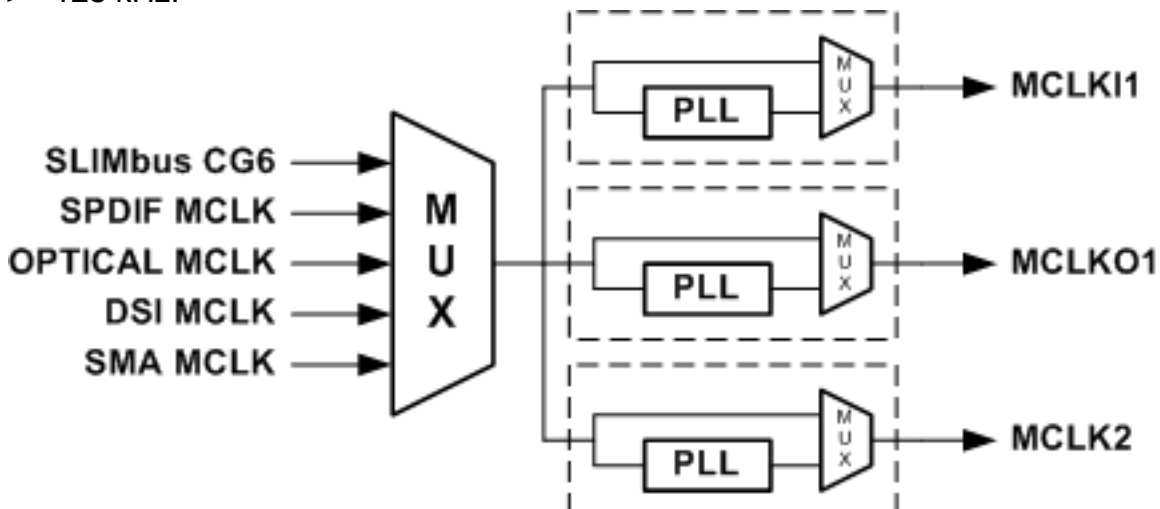
In some cases, the PLL can be automatically bypassed:

- the PLL reference clock frequency is equal to the desired clock frequency
- the desired clock frequency can be derived from the PLL reference clock by an integer divider

This feature can be useful to avoid the jitter generated by the PLL or to be able to inject an “on purpose” jittered clock signal.

4.2. Audio Master Clock Generation

The audio master clock corresponds to $256 \times F_s$ when $F_s < 128$ kHz and $128 \times F_s$ when $F_s \geq 128$ kHz.



The audio master clocks can be generated by using five input clocks. Note that the three audio clock domains are all derived from a common clock reference (through a PLL or direct division).

The default clock reference is the SLIMbus bus clock as if it was running at Clock Gear 6. This option is therefore only usable as long as the bus Clock Gear is greater or equal to 6. If the bus runs in Clock Gear 5 or less, the PLL cannot be used anymore with the SLIMbus as a reference.

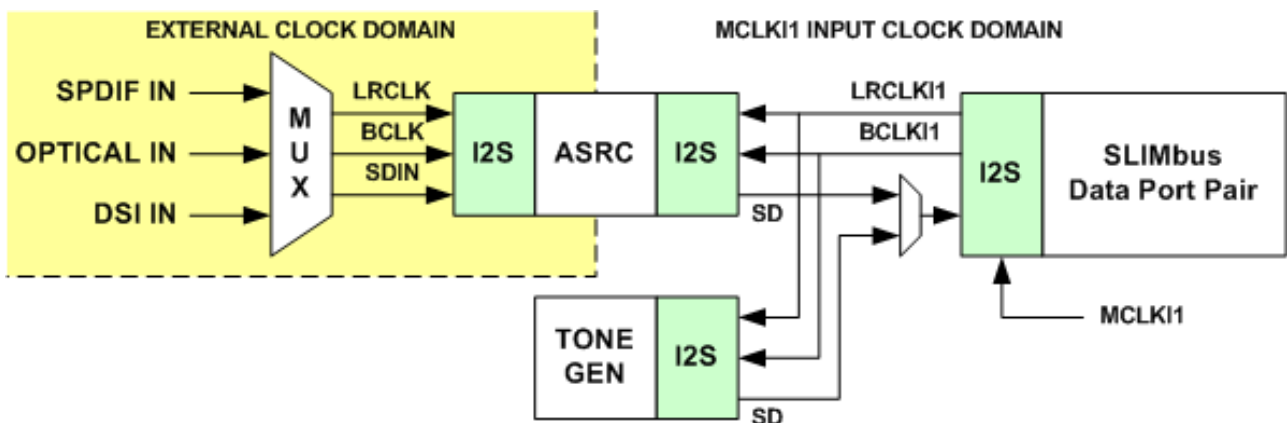
If the audio sample rates are not related to the SLIMbus clock (use of the Pushed or Pulled protocol, for instance), an external master clock shall be used. It can be any of the four other ones:

- SPDIF input recovered master clock
- Optical input recovered master clock
- DSI master clock input on pin 15 of the DSI connector
- External clock on the SMA connector

It is also possible to use the sample rate converters but they will add their own contribution to the signal (delay, frequency response ripple and time domain ringing). The sample rate converters are provided for convenience but they shall not be used when the aim of the test is to characterise the Device Under Test audio performances.

4.2.1. Input Clock Domain 1 (MCLKI1)

The following figure shows the block diagram of the clock domain 1 inputs.

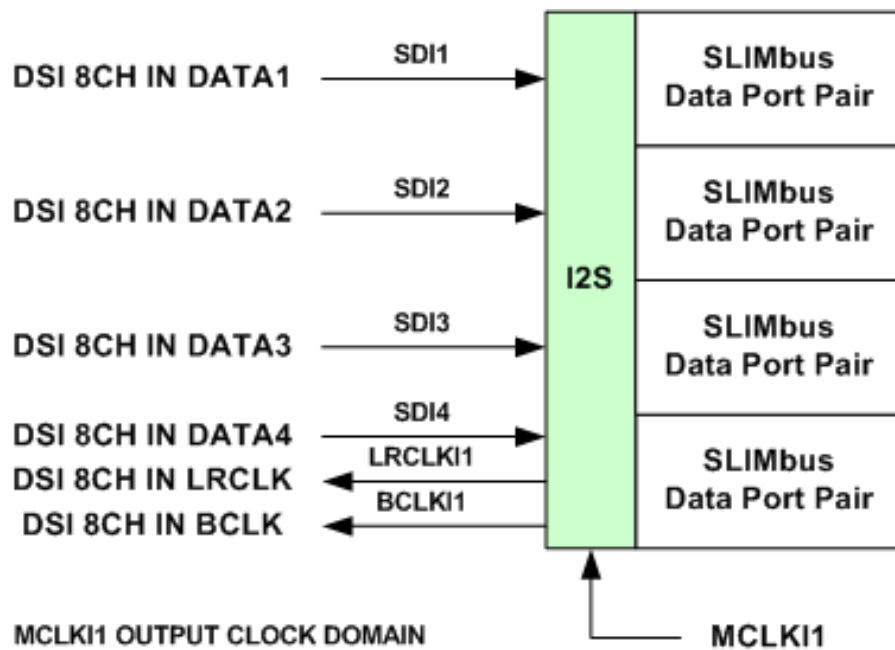


The SPDIF and Optical inputs have their own clock domain. The use of an ASRC appears to be necessary if the audio master clock MCLKI1 is not generated from the SPDIF or Optical clocks.

The DSI input may also have its own clock domain when the interface is set as a clock slave. However, when the DSI input is set as clock master, the DSI input uses the audio master clock MCLKI1 (clock domain 1) as reference.

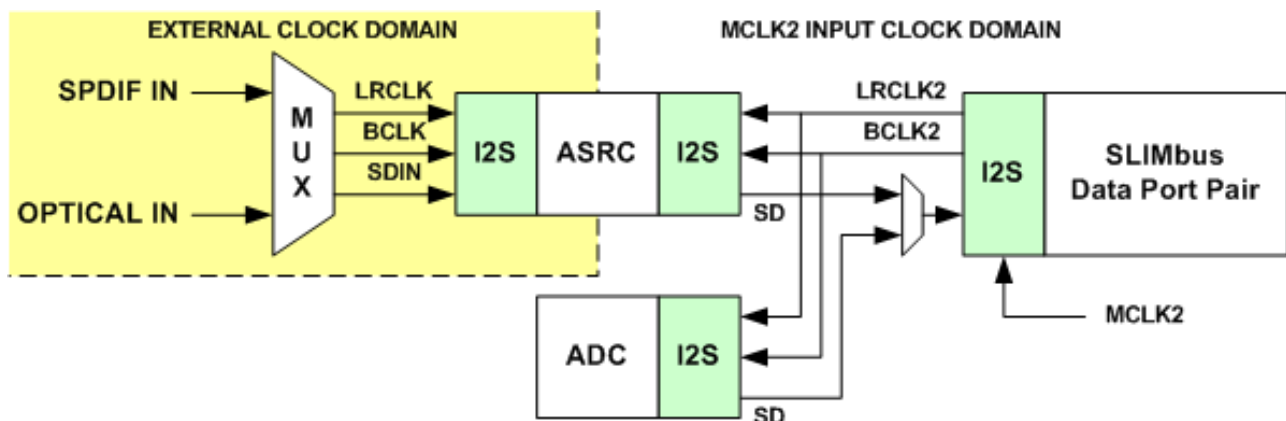
Note that the bridge tone generator is always using the audio master clock MCLKI1 as a reference.

When using the DSI 8 Channel input mode, the interface is clock master and depends entirely on the MCLKI1 clock domain.



4.2.2. Input Clock Domain 3 (MCLK2)

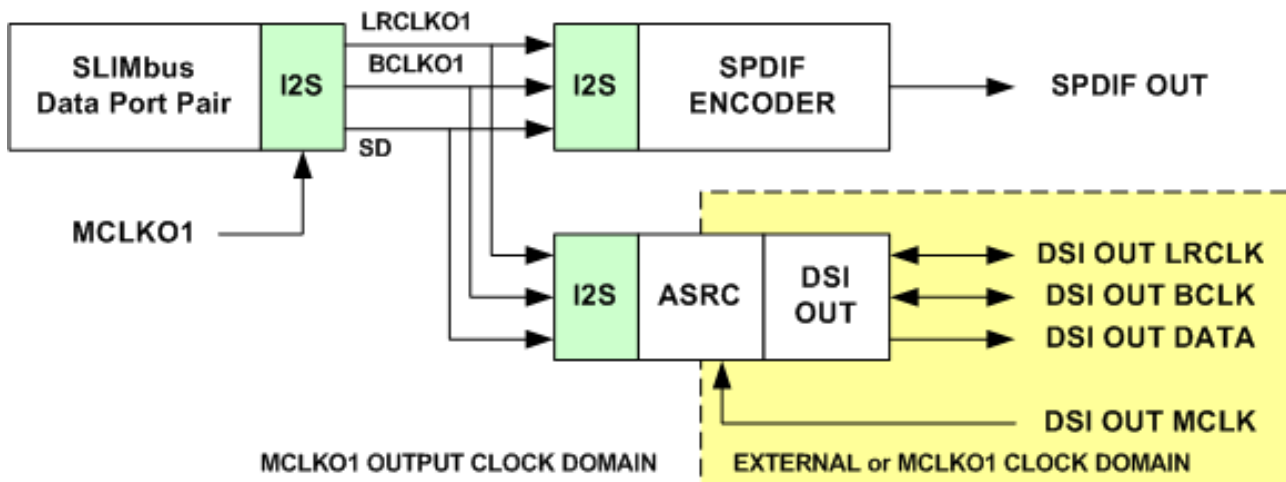
The following figure shows the block diagram of the clock domain 3 inputs. It is very similar to the clock domain 1 inputs with the exception that there is no DSI interface available in this group.



Note that the analogue to digital converter (ADC) is always using the audio master clock MCLK2 as a reference.

4.2.3. Output Clock Domain 2 (MCLK01)

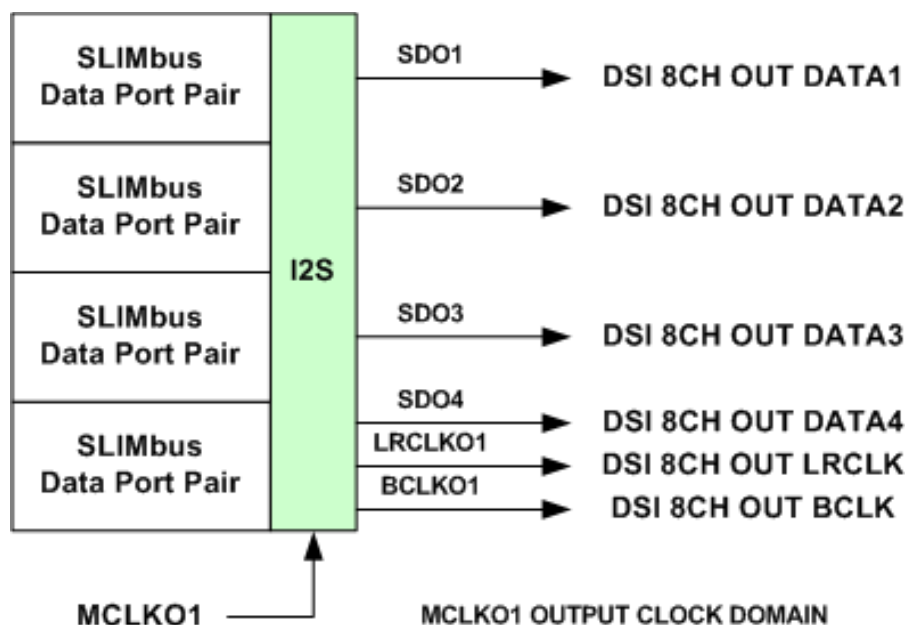
The following figure shows the block diagram of the clock domain 2 outputs.



The SPDIF output is always belonging to the internal clock domain 2. The DSI output can operate in different configuration. The following table lists the configurations that will not generate any audio stream disturbances.

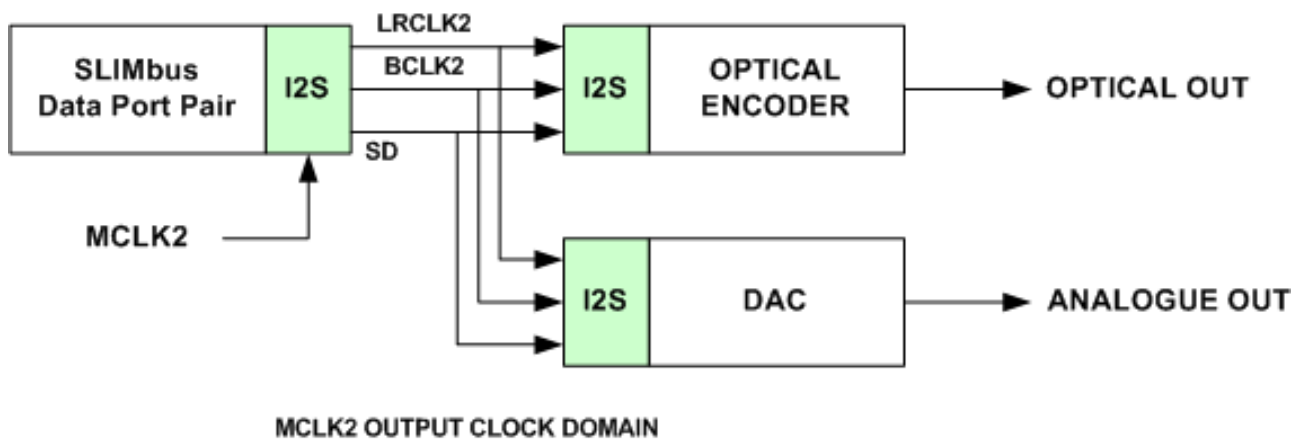
Clock Mode	ASRC	Clock domain
Master	OFF	MCLKO1
Master	ON	DSI OUT MCLK
Slave	ON	DSI OUT MCLK

When using the DSI 8 Channel output mode, the interface is clock master and depends entirely on the MCLKO1 clock domain.



4.2.4. Output Clock Domain 3 (MCLK2)

The following figure shows the block diagram of the clock domain 3 outputs.



Both outputs are slaved to the bridge clock domain 3.

4.3. Common Frequencies

The following table lists the cardinal frequencies that are likely going to be used with the bridge. Note that the bridge makes a best estimate of the measured frequencies by comparing the measured value to the commonly used frequencies and use that estimated value to program the PLLs.

Do not feed the bridge with an arbitrary frequency that does not relate in anyway to the frequencies listed in the table. The PLL generated frequencies might not be as accurate as necessary.

Root Frequency	PLL Generated	Externally Fed
RF=0 ("Not Indicated")	Not Possible	Any frequency
RF=1 (24,576 MHz)	24,576 MHz	24,576 MHz
RF=2 (22,5792 MHz)	22.578998 MHz (Error of -202 Hz)	22,5792 MHz
RF=3 (15,36 MHz)	15,36 MHz	15,36 MHz
RF=4 (16,8 MHz)	16,8 MHz	16,8 MHz
RF=5 (19,2 MHz)	19,2 MHz	19,2 MHz
RF=6 (24 MHz)	24 MHz	24 MHz
RF=7 (25 MHz)	25 MHz	25 MHz
RF=8 (26 MHz)	26 MHz	26 MHz
RF=9 (27 MHz)	27 MHz	27 MHz

5. SLIMbus Operations

The bridge will operate accordingly to the SLIMbus specification.

5.1. Device Enumeration

After the boot sequence, the bridge will send 3 REPORT_PRESENT messages. The Instance Value (IV) of the Enumeration Address depends on the value given to the Component address.

Component address = 0

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0002	0x00	0x00	0x01C100020000
Framer	0x01C1	0x0002	0x01	0x00	0x01C100020100
Generic	0x01C1	0x0002	0x02	0x00	0x01C100020200

Component address = 1

Device	MID	PID	DI	IV	Enumeration Address
Interface	0x01C1	0x0002	0x00	0x01	0x01C100020001
Framer	0x01C1	0x0002	0x01	0x01	0x01C100020101
Generic	0x01C1	0x0002	0x02	0x01	0x01C100020201

5.2. Channel Setup

When using the PLLs to generate the audio clocks, some care must be taken to ensure optimal data transmission and / or reception.

The PLLs are configured once the associated Presence Rate is known. The SLIMbus Core communicates that information to the controller when a port is configured and when the associated channel structure and content have been defined by a valid reconfiguration sequence. Note that the channel does not need to be active yet to get the bridge to configure itself for the audio operation.

Once the PLLs are configured and stable (it takes less than 3 ms), the channel can be activated and the data streaming will start without any latency or loss of data.

The sequence of message will be as follow:

*** CONNECT_SOURCE or CONNECT_SINK messages ***

BEGIN_RECONFIGURATION

NEXT_DEFINE_CHANNEL(...)

NEXT_DEFINE_CONTENT(...)

RECONFIGURE_NOW

...

<--- At that moment, the PLLs get configured

*** Delay for 3 ms ***

...

BEGIN_RECONFIGURATION
NEXT_ACTIVATE_CHANNEL(...)
RECONFIGURE_NOW

... <--- The data streaming is effectively starting

If the channel activation message is in the channel setup sequence, there will be a delay of about 3 ms during which the data will either not be transmitted on the bus or not be read. When dealing with audio tests, it is definitively not an issue. When it is about verifying that every sample sent is well received, special care must be taken.

Deactivating a channel does not reset the PLL settings. Therefore, the channel can be reactivated at any time and be immediately operational. Only a port reset (through a DISCONNECT_PORT or REMOVE_CHANNEL messages) will affect the PLL configuration.

Note that these recommendations will not apply when an external clock source is used, as the audio clocks are required to be present and stable before the audio channel is activated.

5.3. ASRC Configuration

The bridge uses the DL field (Data Length) to adequately set the output word length of the asynchronous sample rate converter. Dithering is applied on the LSB of the sample for optimal THD+N performances. The data lengths of interest are 16 bits (4 slots), 20 bits (5 slots) and 24 bits (6 slots). 32 bits data length is not an option when using the ASRCs.

If the DL field is smaller than 4 slots, the ASRC output word length will be set by default to 16 bits. If the DL field is greater than 6 slots or set to "Not Indicated", the output word length will be set by default to 24 bits.

The data length is specified by the Data Length field value in the NEXT_DEFINE_CONTENT message. Make sure that the data Segment is large enough to fit the sample as defined by the DL field. Otherwise, the dithered bit will be lost and the sample truncation will lead to undesired distortions.

If the ASRC is not activated, the DL field value will not have any effect on the bridge behaviour.

5.4. Audio Data Format

The bridge supports 2 audio data formats:

- DT=0 ("Not Indicated") forces the bridge to use the 2's complement data format.
- DT=1 ("LPCM") forces the bridge to use the sign&offset magnitude format defined by the SLIMbus specification. It will convert 2's complement samples to LPCM and vice&versa.

The data format is specified by the Data Type field value in the NEXT_DEFINE_CONTENT message.

5.5. Using the Value Elements to configure the Bridge

Most of the bridge parameters can be modified by using the Value Elements of the Generic device. To validate the bits set in the Value Element, the most significant bit (b7) of the Value Element must be set. Otherwise the Value Element content will not have any other effect than being displayed in the Bus Status page.

The bit assignment is shown in the following tables.

	Bit	Name	Description
V E 0	0	INPUT1_SEL0	Select the signal source of the ports 0 to 7. 0 = SPDIF, 1 = Optical, 2 = DSI, 3 = Tone Generator.
	1	INPUT1_SEL1	
	2	INPUT1_SEL3	Select signal source of the ports 3 to 7 (0 = copy P1-P4, 1 = tone gen)
	3	INPUT2_SEL0	Select the signal source of the ports 8 to 11. 0 = SPDIF, 1 = Optical, 2 = Analogue.
	4	INPUT2_SEL1	
	5	INPUT1_ASRC_ENA	Activate the Asynchronous Sample Rate Converter of the input 1 group
	6	INPUT2_ASRC_ENA	Activate the Asynchronous Sample Rate Converter of the input 2 group
	7	VE0_VALIDATE	Activate the functions of bit 0 to 6 when set to 1

VE0 of the Generic Device at address 0x800

	Bit	Name	Description
V E 1	0	OUTPUT1_SEL0	Select the port pair to be output on SPDIF and DSI outputs
	1	OUTPUT1_SEL1	
	2	DSI_8CH_ENA	Enable 8 CH mode on the DSI interface
	3	DSI_8CH_MODE	Set the DSI interface as input (0) or output (1)
	4	OUTPUT2_SEL	Select the port pair to be output on Optical and analogue outputs
	5	DSI_OUT_ASRC_ENA	Activate the Asynchronous Sample Rate Converter of the DSI output
	6	DSI_OUT_ASRC_CLK	Select the DSI output ASRC master clock (0= DSI, 1 = MCLKO1)
	7	VE1_VALIDATE	Activate the functions of bit 0 to 6 when set to 1

VE1 of the Generic Device at address 0x801

	Bit	Name	Description
V E 2	0	LOOPBACK_ENA	Data loop back functionality. Enabled when set to 1
	1	DAC_ATTN0	DAC output attenuation level in dB It ranges from 0 dB to 62 dB by step of 2 dB
	2	DAC_ATTN1	
	3	DAC_ATTN2	
	4	DAC_ATTN3	
	5	DAC_ATTN4	
	6	EXT_CLK_ZIN_SEL	Set the input clock impedance (0 = 1M, 1 = 50R)
	7	VE2_VALIDATE	Activate the functions of bit 0 to 6 when set to 1

VE2 of the Generic Device at address 0x802

	Bit	Name	Description
V E 3	0	DSI_LEVEL0	Select the DSI signaling level 0 = 1V8, 1 = 2V5, 2=3V3
	1	DSI_LEVEL1	
	2	DSI_IN_FORMAT	Set the Stereo DSI input format (0 = L-J, 1 = I2S)
	3	DSI_IN_CLK_MODE	Set the DSI IN Master/Slave clock mode (0 = Slave, 1 = Master)
	4	DSI_OUT_FORMAT	Set the Stereo DSI output format (0 = L-J, 1 = I2S)
	5	DSI_OUT_CLK_MODE	Set the DSI OUT Master/Slave clock mode (0 = Slave, 1 = Master)
	6	EXT_CLK_DIR	Set the external clock direction (0 = input, 1 = output)
	7	VE3_VALIDATE	Activate the functions of bit 0 to 6 when set to 1

VE3 of the Generic Device at address 0x803

	Bit	Name	Description
V E 4	0	EXT_CLK_LEVEL0	Select the external clock signaling level 0 = 1V8, 1 = 2V5, 2=3V3
	1	EXT_CLK_LEVEL1	
	2	CLK_OUT_SRC0	Select the clock to be output on the external clock connector 0 = Framer, 1 = MCLKI1, 2 = MCLKO1, 3 = MCLK2
	3	CLK_OUT_SRC1	
	4	AUDIO_PLL_REF0	Select the audio PLL clock reference 0 = SLIMbus, 1 = SPDIF IN, 2 = OPRICAL IN, 3 = DSI MCLK, 4 = SMA
	5	AUDIO_PLL_REF1	
	6	AUDIO_PLL_REF2	
	7	VE4_VALIDATE	Activate the functions of bit 0 to 6 when set to 1

VE4 of the Generic Device at address 0x804

6. Tone Generator Characteristics

The internal tone generator offers basic signals for quick and simple tests. It has 2 independent channels. Not that the generator has not been designed to fulfil all the duties of a fully featured audio analyzer.

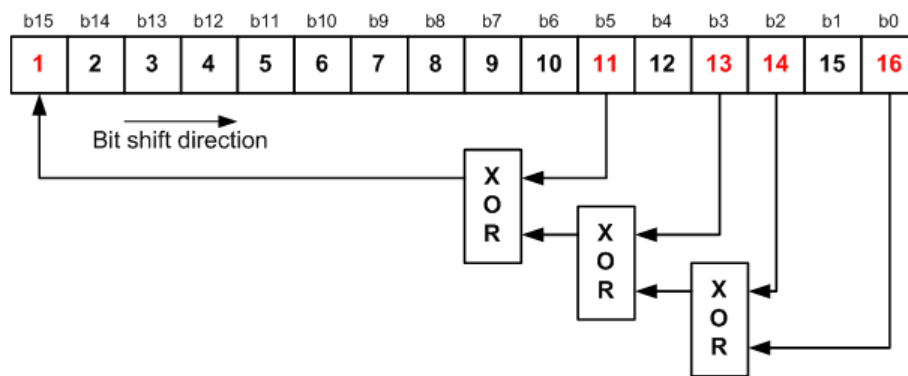
The generator offers signals for all the sampling rates, from 8 kHz up to 384 kHz.

There are 3 signals available:

- A 32 bits constant (DC) value (per channel)
- A Pseudo Random Bit Sequence (common to both channels)
- A sine wave with selectable frequencies and amplitude (per channel).

6.1. Pseudo Random Bit Sequence

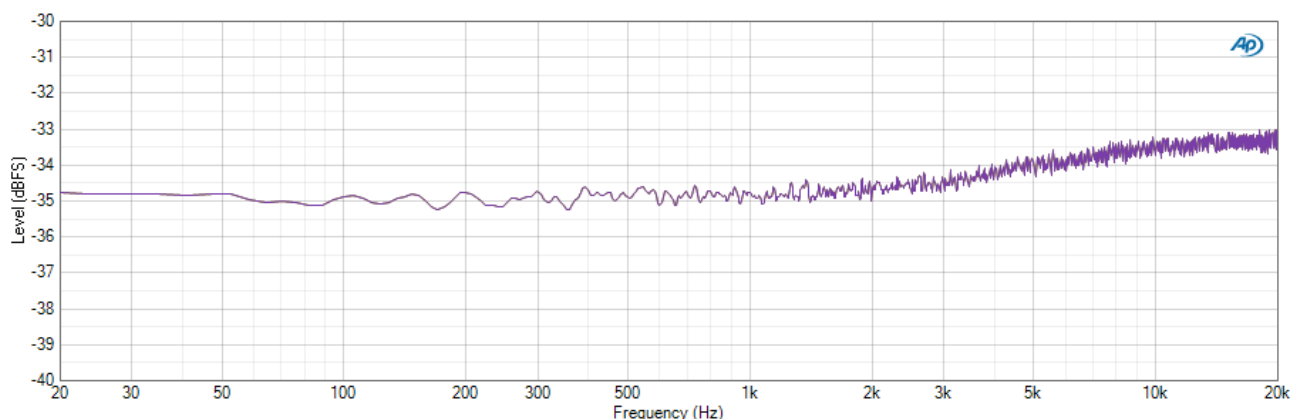
The PRBS generator is based on a 16 bits linear feedback shift register (LFSR). The polynomial is equal to $X^{16}+X^{14}+X^{13}+X^{11}+1$ (Fibonacci implementation).



The 32 bit sample is built with 2 copies of the LFSR:

- Sample[31:16] = 2^{14} -LSRF
- Sample[15:0] = 2^{14} -LSFR
-

The constant value 2^{14} has been added to flatten the noise spectrum density. There is a small 1.5 dB rise from $F_s/48$ till $F_s/2$.



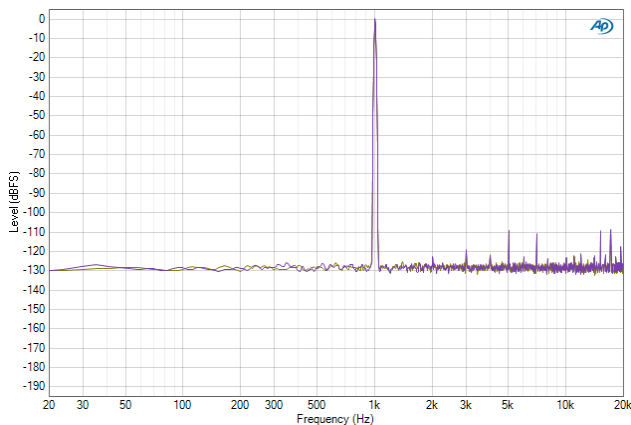
Noise spectrum at a sampling rate of 48 kHz

The LFSR cycle length is equal to $2^{16}-1$ (65535). The LFSR is initialised with the value 0x0001.

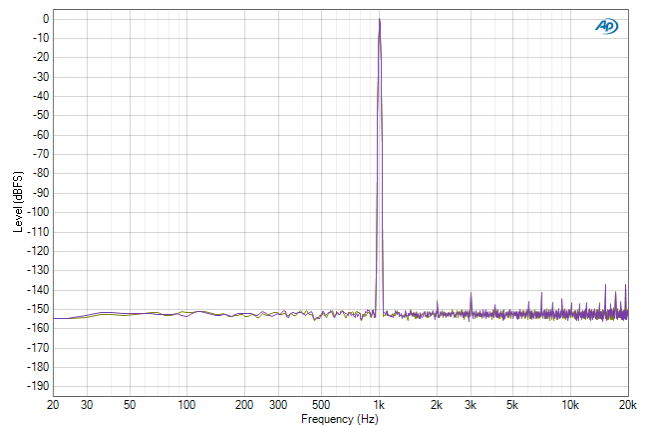
6.2. Sine Wave

The waveforms are built on a look-up table. The possible tone frequencies are given by the formula $F_t = F_s \times N / 3072$. At $F_s = 48$ kHz, the frequency step is equal to 15.625 Hz. Dithering is applied to the samples at the appropriate location, depending on the Data Length information provided in the NEXT_DEFINE_CONTENT message that defined the data channel in use.

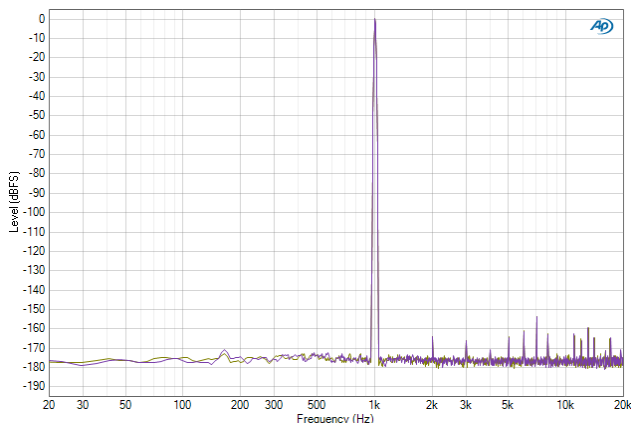
The following plots show a 1 kHz sine wave @ 0 dBFS and $F_s=48$ kHz. Even if not absolutely perfect, the signal purity is excellent (see the THD+N figures).



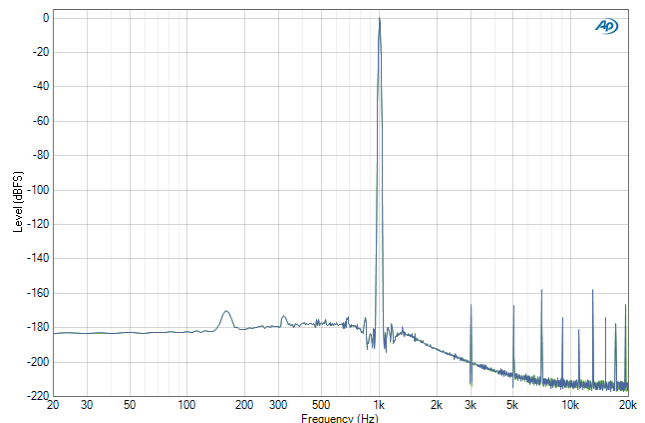
16 bits, THD+N = -95.5 dB



20 bits, THD+N = -120.2 dB



24 bits, THD+N = -143.8 dB



32 bits, THD+N = -152.9 dB

7. Electrical Specifications

Power Supply

Parameter	Min	Typical	Max	Unit
Power supply voltage	9		12	V
Operating power			6	W
Standby power	2.2			W

DSI Interface

Parameter	Min	Typical	Max	Unit
DSI OUT signaling voltage (output)	1.8		3.3	V
DSI OUT signaling voltage (input)	1.5		3,6	V
Input pin capacitive load			15	pF
Master clock frequency	2		24.576	MHz
Word clock frequency	8		384 ⁽¹⁾	kHz
Bit clock frequency	512		12.288	MHz

(1) 384 kHz when the 8 channel DSI mode is used. 192 kHz in stereo mode.

SPDIF IN /OUT Interface

Parameter	Min	Typical	Max	Unit
SPDIF IN signaling voltage		1		Vpp
SPDIF IN impedance		75		Ohms
SPDIF OUT signaling voltage		1		Vpp
SPDIF OUT impedance		75		Ohms
Sample Rate (input and output)	20		192	kHz

OPTICAL IN /OUT Interface

Parameter	Min	Typical	Max	Unit
Sample Rate (input and output)	20		96	kHz

External Clock (SMA)

Parameter	Min	Typical	Max	Unit
Signaling voltage (input), Vclk =1.8V, 2.5V or 3.3V	1.5V		VDD+0.3	V
Signaling voltage (output)	1.8V		3.3	V
Input impedance	50		1M	Ohms
Frequency			25	MHz

Analogue Output

Parameter	Min	Typical	Max	Unit
Full scale output level		1		Vrms
Output impedance	100			Ohms
Bandwidth (-3dB)	3,8		0,546xFs or 20k	Hz
Frequency Response Flatness			0,05	dB
THD+N (0dBFS, 20kHz BW)			0,002	%
Dynamic Range		102		dB

Analogue Input

Parameter	Min	Typical	Max	Unit
Input level (@ -0.5 dBFS)		1		Vrms
Input impedance			47k	Ohms
Bandwidth (-3dB)	0.9		0,546xFs or 20k	Hz
Frequency Response Flatness			0,05	dB
THD+N (full scale, 20kHz BW)			0,003	%
Dynamic Range		99		dB

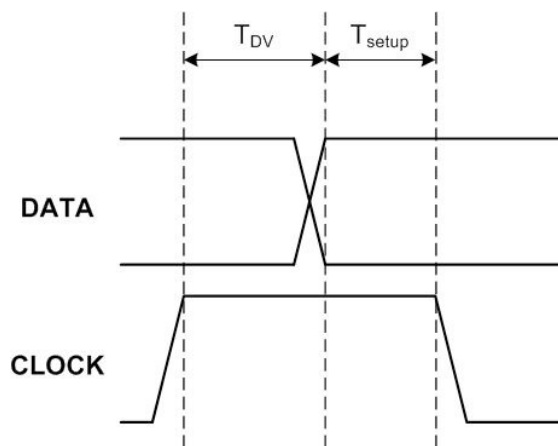
ASRC performances

Parameter	Min	Typical	Max	Unit
THD+N (0dBFS, 24 bits resolution)			-140	dB
Dynamic Range		142		dB
Input / Output Sampling Ratio	1:16		16:1	

SLIMbus Electrical Performances

Parameter	Min	Typical	Max	Unit
Clock Gear range	1		10	
Operating frequency			27	MHz
Signaling voltage	0.9		3.3	V
Bus Hold impedance		33		kOhms
Clock and Data output impedance		15		Ohms
Clock and Data input capacitive load			20	pF

SLIMbus Timing specifications



With Internal Framer:

$$T_{DV} > 2 \text{ ns}$$

$$T_{DV} < 7.2 \text{ ns}$$

With External Framer:

$$T_{DV} < 12 \text{ ns}$$