SoundWire Analyzer

User Manual

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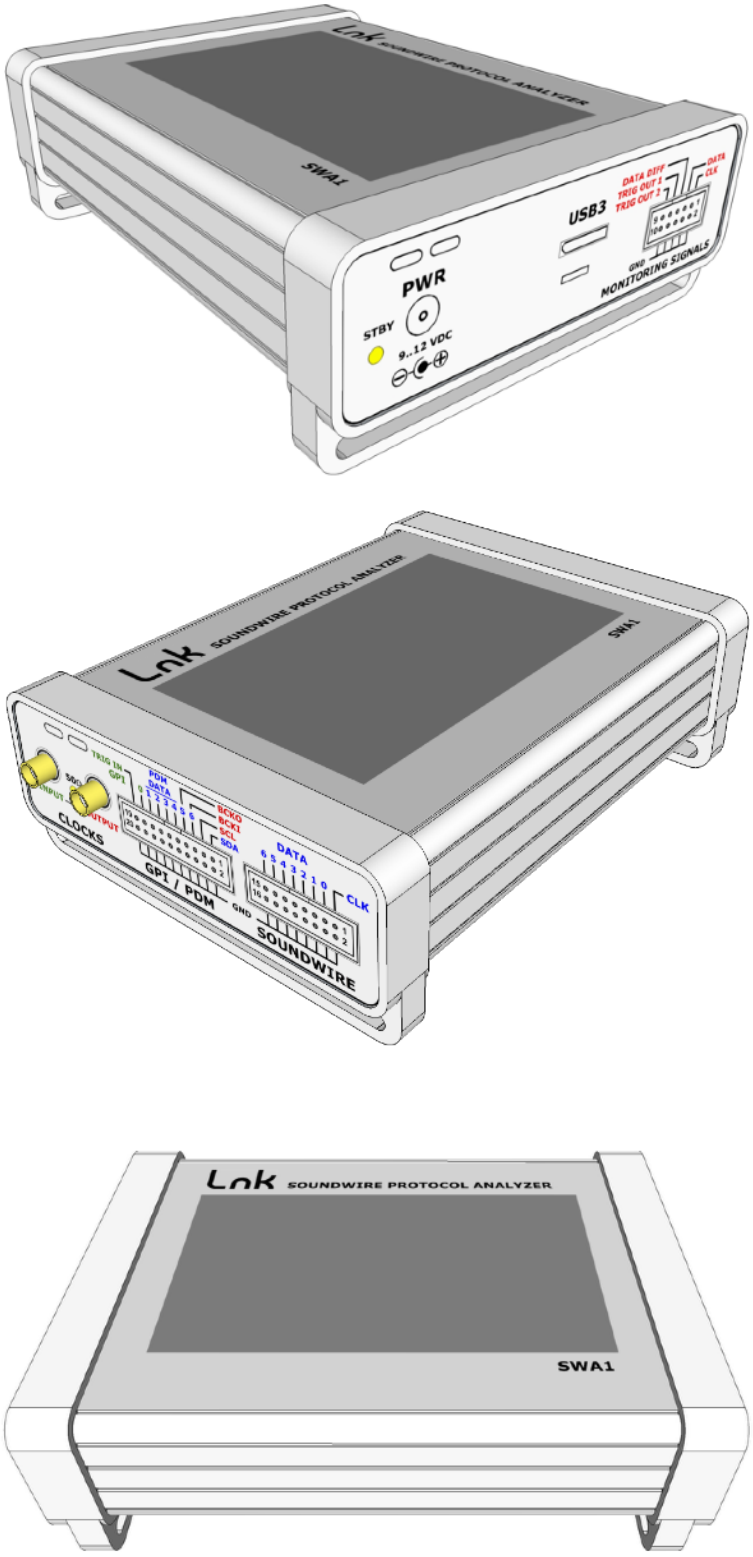
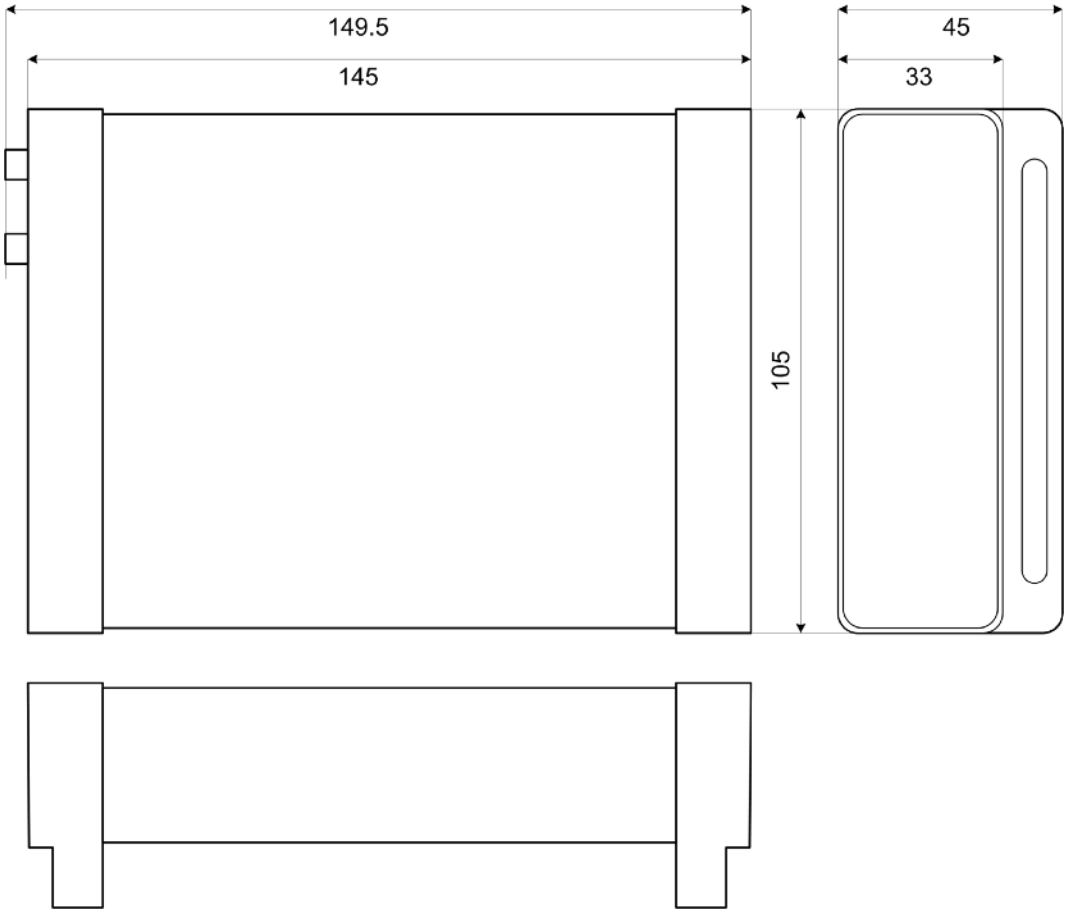
1. HARDWARE SPECIFICATION



1.1. Hardware dimension



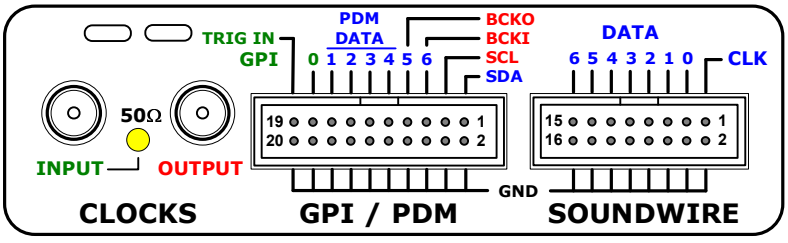
All dimensions are in millimetres.
Unit weight : 490 g.
Body material: anodised aluminium.

1.2. User Interface

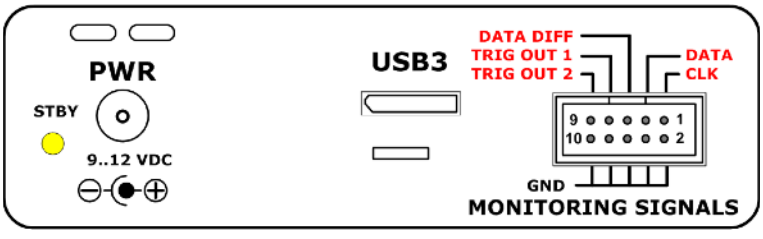
All the hardware controllable features are accessible through the 4.3” colour touch screen of the unit.

1.3. Connectivity

The unit has multiple connectors located on the left side and on the right side.



(left)

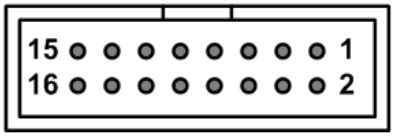


(right)

1.3.1. SoundWire bus connector

The SoundWire signals (clock and data) are available on a boxed IDC 16 pin header connector with a regular pitch of 2.54 mm (0.1”). The bottom pins are all connected to ground.

Pin	Signal	Direction
1	Clock	Input & output
3	Data Line 0 (main)	Input & output
5	Data Line 1	Input & output
7	Data Line 2	Input & output
9	Data Line 3	Input & output
11	Data Line 4	Input & output
13	Data Line 5	Input & output
15	Data Line 6	Input & output
2..16	Ground	



The data line bus keepers cannot be controlled individually. Either all ON or all OFF.

Electrical Parameter	Min	Nominal	Max	Units	Remarks
SoundWire signaling level	0.9	1.8	3.2	V	Programmable by steps of 50 mV
Bus Keeper impedance	6950		1M	Ohms	Bus keeper can be deactivated
Output impedance	15			Ohms	
Input impédance		1M		Ohms	When Bus Hold is disabled

1.3.2. Multi-purpose connector

The signals (clock and data) are available on a boxed IDC 20 pin header connector with a regular pitch of 2.54 mm (0.1”). The bottom pins are all connected to ground.
This connector serves multiple purposes. It features an I2C interface that can either acts as a slave or as a master (not implemented yet). There is a dedicated trigger input pin. Six of the seven general purpose input pins can be reassigned to a multichannel PDM input & output interface or a multichannel PCM input or output.

Electrical Parameter	Min	Nominal	Max	Units	Remarks
GPI & I2C signaling level	0.9		3.2	V	Programmable by steps of 50 mV
Output impedance	47			Ohms	
Input impédance		47k		Ohms	

	FUNCTION							
Pin	**GPI**		**PDM 8 CH IN**		**PDM 4 IN / 4 OUT**		**PDM 8 CH OUT**	
1	I2C_SDA	I/O	I2C_SDA	I/O	I2C_SDA	I/O	I2C_SDA	I/O
3	I2C_SCL	I/O	I2C_SCL	I/O	I2C_SCL	I/O	I2C_SCL	I/O
5	GPI6	IN	PDM_BCKI	OUT	PDM_BCKI	OUT	PDM_BCKI	OUT
7	GPI5	IN	PDM_BCKO	OUT	PDM_BCKO	OUT	PDM_BCKO	OUT
9	GPI4	IN	PDM_DATA4	IN	PDM_DATA4	OUT	PDM_DATA4	OUT
11	GPI3	IN	PDM_DATA3	IN	PDM_DATA3	OUT	PDM_DATA3	OUT
13	GPI2	IN	PDM_DATA2	IN	PDM_DATA2	IN	PDM_DATA2	OUT
15	GPI1	IN	PDM_DATA1	IN	PDM_DATA1	IN	PDM_DATA1	OUT
17	GPI0	IN	GPI0	IN	GPI0	IN	GPI0	IN
19	TRIG IN	IN	TRIG IN	IN	TRIG IN	IN	TRIG IN	IN
2..20	Ground							

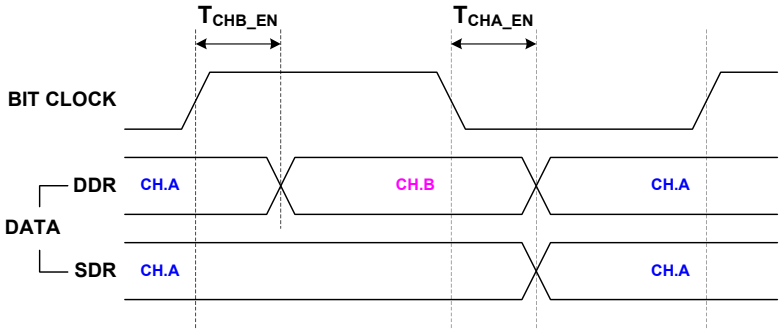
	FUNCTION			
Pin	**PCM 8 CH IN**		**PCM 8 CH OUT**	
1	I2C_SDA	I/O	I2C_SDA	I/O
3	I2C_SCL	I/O	I2C_SCL	I/O
5	PCM_BCLK	OUT	PCM_BCLK	OUT
7	PCM_LRCLK	OUT	PCM_LRCLK	OUT
9	PCM_DATA4	IN	PCM_DATA4	OUT
11	PCM_DATA3	IN	PCM_DATA3	OUT
13	PCM_DATA2	IN	PCM_DATA2	OUT
15	PCM_DATA1	IN	PCM_DATA1	OUT
17	GPI0	IN	GPI0	IN
19	TRIG IN	IN	TRIG IN	IN
2..20	Ground			

1.3.2.1. GPI operation

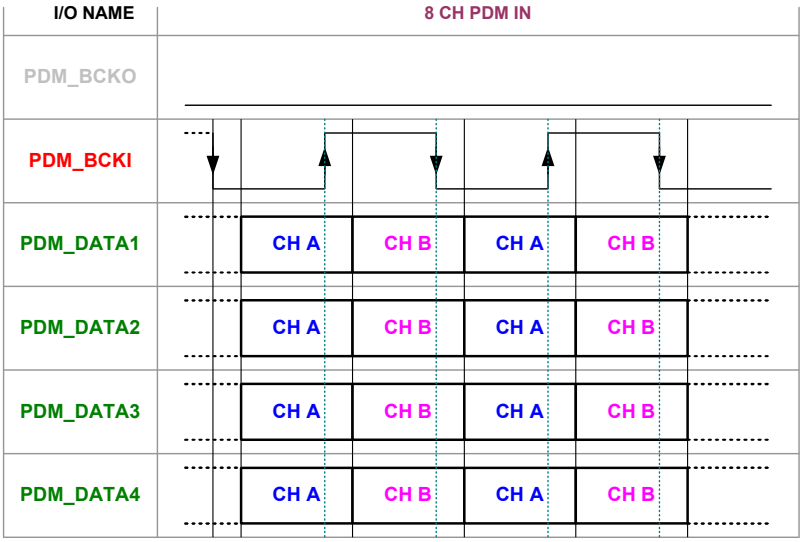
The GPI pin logical levels are all sampled by the analyzer at the beginning of every frame. The captured value are shown in the analyzer traces.

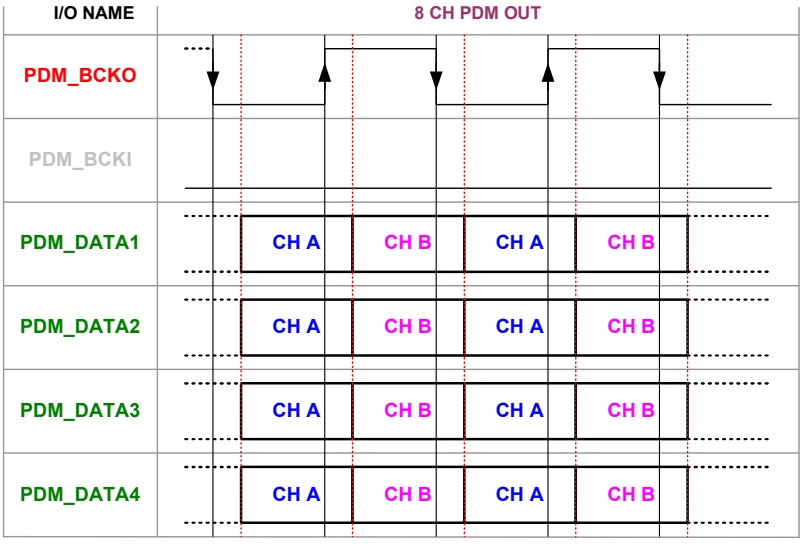
1.3.2.2. Serial Audio Interface

The interface is always a clock **master** because clocks are either directly derived from the SoundWire bus clock or generated from an external audio master clock. The Serial Audio Interface supports PDM and PCM streaming on up to 4 data lines.

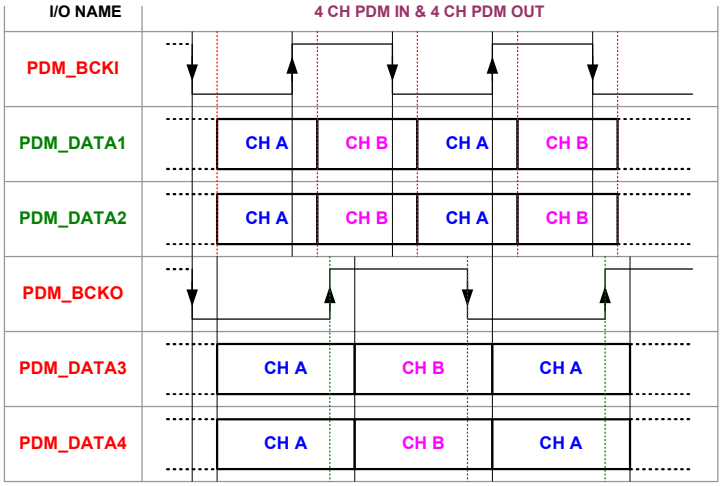


The interface can operate in a single data rate mode (PDM and PCM) or in dual data rate mode (PDM only).
In single data rate mode (SDR), the data is set after the falling edge of the bit clock. The delay between the clock falling edge and the data edge (T_{CHA_EN}) is equal to **13.6 ns**. The data line is sampled on the clock rising edge.
In dual data rate mode (DDR), the data is set after every clock edge (falling or rising). The delay between the clock falling edge and the data edge (T_{CHA_EN}) is equal to **13.6 ns**. The delay between the clock rising edge and the data edge (T_{CHB_EN}) is equal to **12.5 ns**. The data line is sampled on the every clock edge.

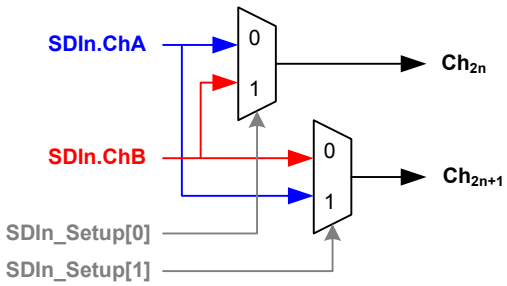




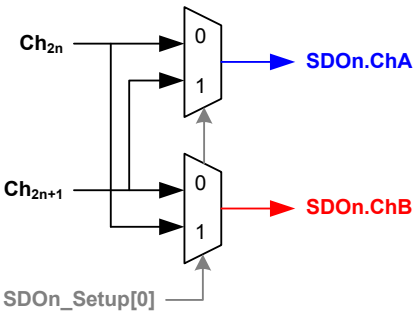
When the Serial Audio Interface is configure to allow both PDM input and output streams, the two bit clocks are totally independent (frequency, phase and time of activation).



The PDM data paths have dedicated routers (one per data line) to increase the data handling flexibility of the interface. See the ScriptBuilder suer manual for the configuration of these data routers.

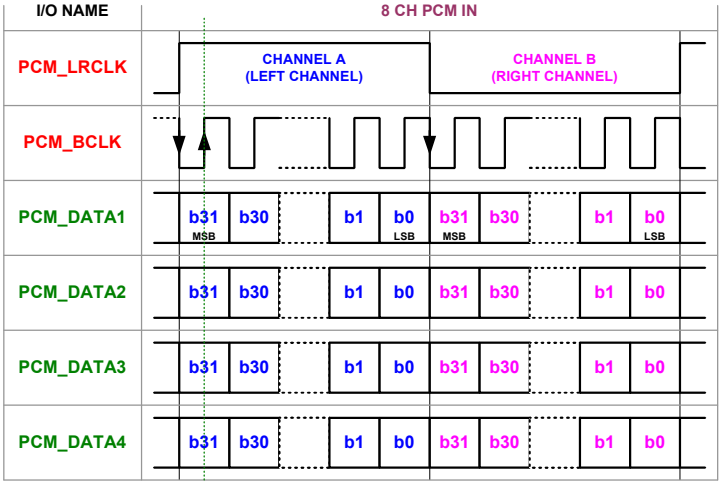


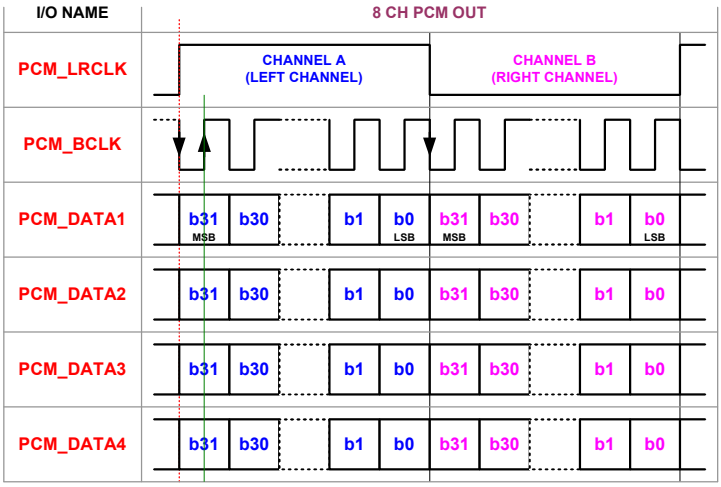
PDM input path



PDM output path

When configured to operate in PCM mode, the interface generates a nit clock and a word clock. The word clock transition always happens on the falling edge of the bit clock. The bit clock is always 64 times greater than the word clock. The data are left aligned, MSB first and each frame channel is 32 bits long.



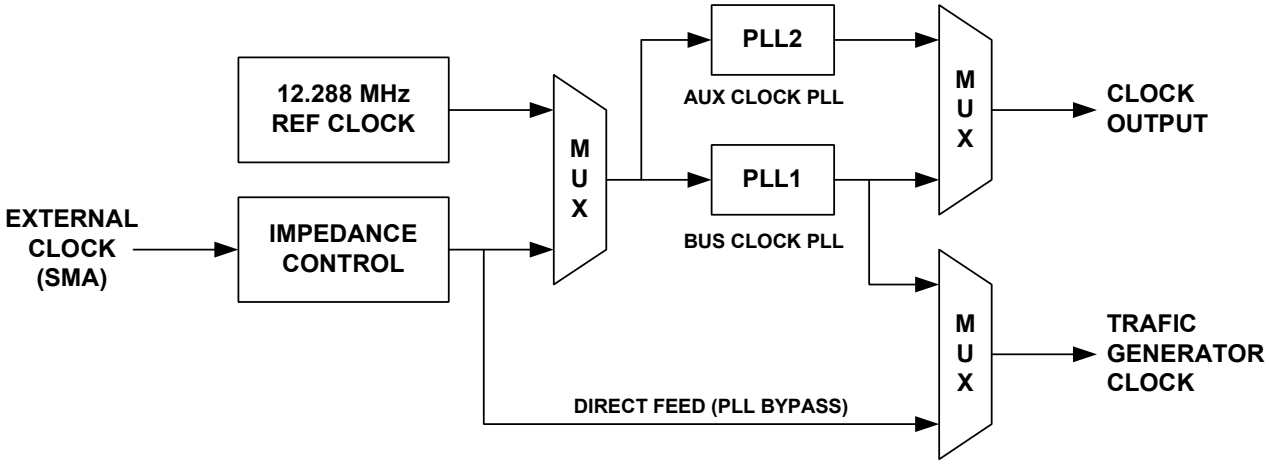


1.3.3. Clock input and output connectors

The unit can input an external clock to feed the SoundWire Traffic Generator. It can also output a configurable clock. The connectors are 50 Ohms SMA.
The input impedance is configurable and can be set to 50 Ohms or 1MOhms. The 50 Ohms state is indicated by a glowing yellow led close to the input connector. The clock signalling level is programmable (from 0.9V to 3.2V by steps of 50mv).

Electrical Parameter	Min	Nominal	Max	Units	Remarks
Clock signaling level	0.9		3.2	V	Programmable by steps of 50 mV
Output impedance		50		Ohms	
Input impédance	50		1M	Ohms	Programmable (50R or 1M)
Input frequency	1		50	MHz	When PLL are used
	0		26	MHz	When using direct feed

The unit has a flexible clock tree.



The traffic generator clock can be generated from a 12.288 MHz high purity oscillator or from an externally fed clock. The PLLs are actually bypassed when the desired frequencies can be derived from the reference clock by an integer divider. If this is not possible, the PLL is used.

It is possible to completely bypass the PLL chip to generate the traffic generator clock. It is therefore possible to proceed with direct injection of clock signals. This is especially interesting when jitter sensitivity tests of frequency variation tests must be performed.

The external input clock can have an arbitrary value. The frequency is measured and the PLLs are configured to generate the desired target frequencies. However, it is always better to use common frequencies for audio and communication system. The unit software will compare the measured frequencies with known values and take the known values that are close (+/- 0.8%) to the measured frequency. This is done to reduce the risk of wrongly set target frequencies. If nothing matches, the PLL parameters will be computed with the measured input frequency value.
When using the PLL, the lowest usable input frequency is 1 MHz.

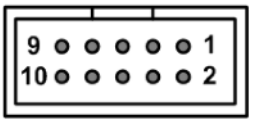
Note: When using direct feed, the external clock frequency **must be twice** the desired SoundWire bus clock (SoundWire clock = 1/2 external clock).

The output clock is fed by one of the two PLL outputs. The Auxiliary clock frequency is manually programmable.

1.3.4. Monitoring Signals connector

The monitoring signals are available on a boxed IDC 10 pin header connector with a regular pitch of 2.54 mm (0.1”). The bottom pins are all connected to ground.

Pin	Signal	Direction
1	Buffered SW clock	Out
3	Buffered SW data	Out
5	DATA DIFF	Out
7	TRIG 1 OUT	Out
9	TRIG 2 OUT	Out
2..10	Ground	



The buffered SoundWire clock signal is a copy of the captured SoundWire clock. It enables scope probing without disturbing the bus. The buffered SoundWire data signal is a copy of one of the 7 SoundWire data lines. The selected line is control through a script command or directly via the PC application.

The Data Diff signal is high every time there is a difference between the transmitted data and the captured data. It indicates where the DUT is writing or if there is a bus clash condition.

The TRIG 1 and TRIG 2 outputs are used to flag specific events happening on the bus. The Trig Out signals are controlled directly by a script command (to spot a specific part of the script) or by an internal event decoder that flags specific events (especially in sniffer mode). The event filter engine is controlled via the PC application.

The monitoring signals use the same signaling level as the GPI/PDM connector.

1.3.5. USB3 connector

The unit needs to be connected to a PC for operation. It does not work as a stand-alone piece of equipment. A USB3 port is required on the PC to properly operate the unit. No power is drawn from the USB3 port. The unit is self powered.

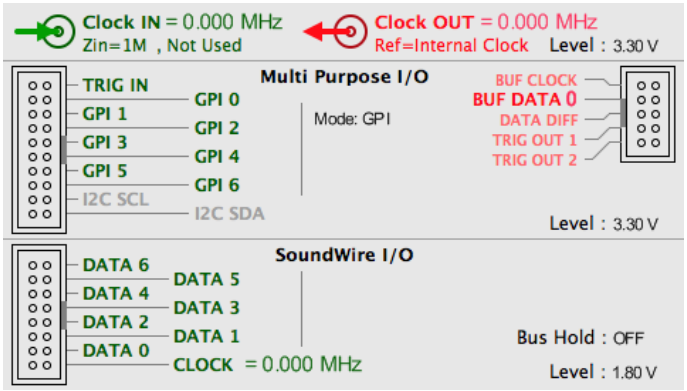
1.3.6. Power supply connector

The unit needs an external supply to operate. The typical supply voltage is 9V. The power consumption depends on many parameters. At a minimum, the unit will consume 1.5 W. If the display is set to maximum brightness and the FPGA is loaded with an IP running a maximum of gates at full speed, the power consumption can reach 5 W.

1.4. Hardware Operation

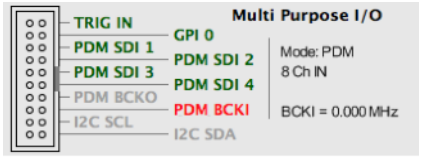
Connect the hardware unit to a USB3 port.
Power on the unit **before** launching the Protocol Analyzer software.

While the unit is waiting for the PC activation, the display will show a standby message asking for PC connection.
Once the Protocol Analyzer software has detected and configured the hardware, the display will show the main page, providing information about the system configuration and the various connector pin functions.

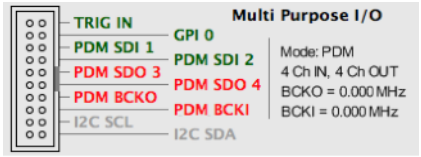


1.4.1. Multi Purpose I/O

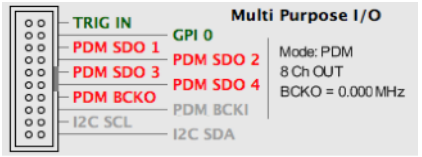
By default, the multi-purpose IOs are configured as input pins. Their state is captured on every frames. When the audio hardware interface option is available, the pins can be configured as serial data lines and clock lines.



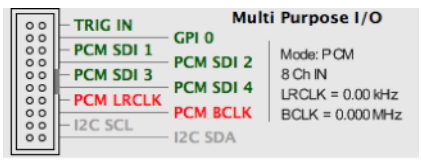
8 Channel PDM inputs



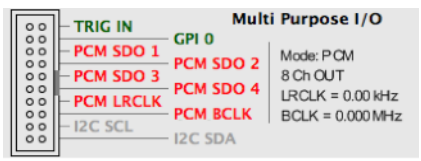
4 Ch PDM in and 4 Ch PDM out



8 Channel PDM outputs



8 Channel PCM inputs



8 Channel PCM outputs

The operation mode is indicated as well as the bit and word clocks (from release 1.27 and upwards).

1.4.2. SoundWire I/O

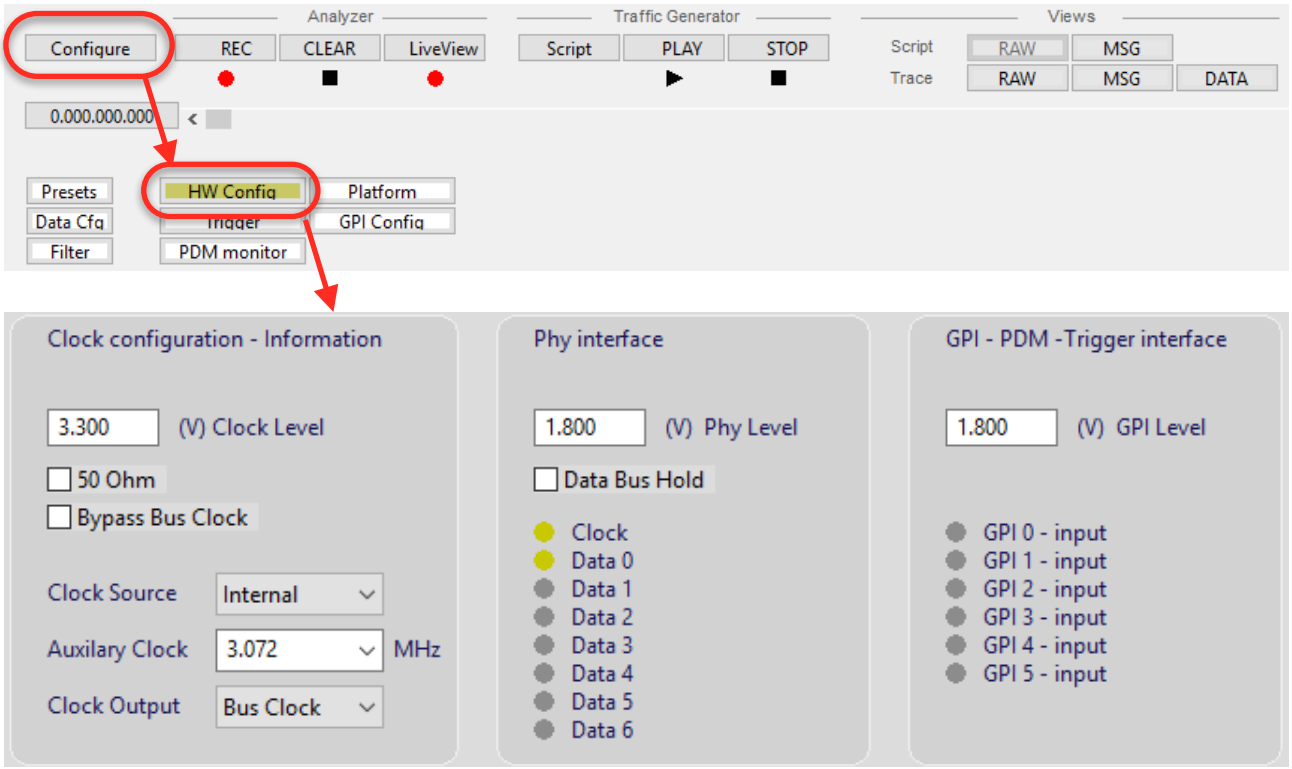
This part of the display shows the measured bus frequency, the status of the bus hold and the SoundWire signalling voltage. When activity is detected on a pin, the display shows a yellow circle in place of the corresponding pin (grey by default).

1.4.3. Clock I/O

The hardware can input a clock signal on a SMA RF connector and output a clock signal on another SMA RF connector.
The display shows the clock IO configuration and functions as well as the measured clocks.

1.5. Hardware Parameter Control

All of these parameters can be controlled by a script, when the tool is used as a traffic generator (see the ScriptBuilder user manual) or in real time by the hardware control panel of the analyser software.

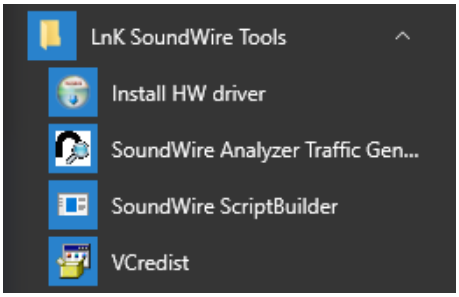


2. SOFTWARE OPERATION

2.1. Installation

Double click on the installation software located on the USB memory stick.
It has a name in the form of LnK_SoundWire_Tools_XXX.exe.
Note that it's always a good practice to copy the latest software release on the provided USB memory stick.

Once the installation is finished, go to the windows menu Program (in the task bar) and select LnK SoundWire Tools.



- Make sure the the HW unit is unplugged from any USB port of the PC.
- Run the Install HW driver application.
- In some cases, it might be required to install the Microsoft redistributable DLLs by running the VCredist application.
- Plug the USB license key (blue dongle) in any of the USB port of the host PC. Drivers installation is not required to operate the license dongle.
- Plug the hardware unit on a USB3 port (preferably) or a USB2 port.

The tools are ready for operation.

2.1. Software units

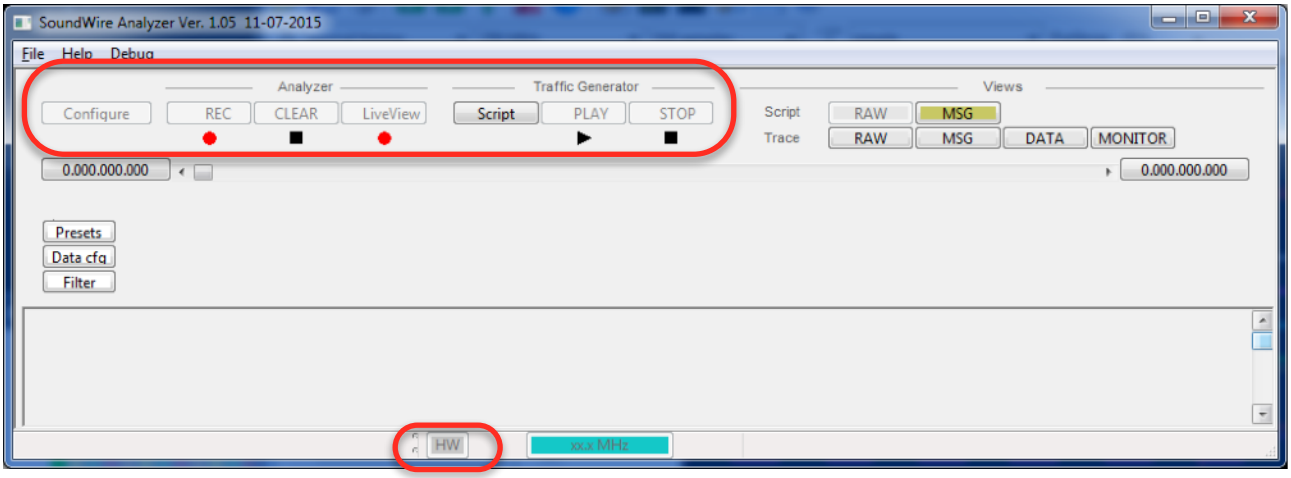
The tool uses 2 softwares:
- The SoundWire Protocol Analyzer & Traffic Generator. The present user manual is dedicated to this piece of software.
- The script editor (named ScriptBuilder) to generate XML scripts to be used by the Traffic Generator. ScriptBuilder also provide a very powerful capture post processing tool. Refer to the ScriptBuilder user manual for detailed explanation on the XML scripting tags.

2.2. Launching the Protocol Analyzer

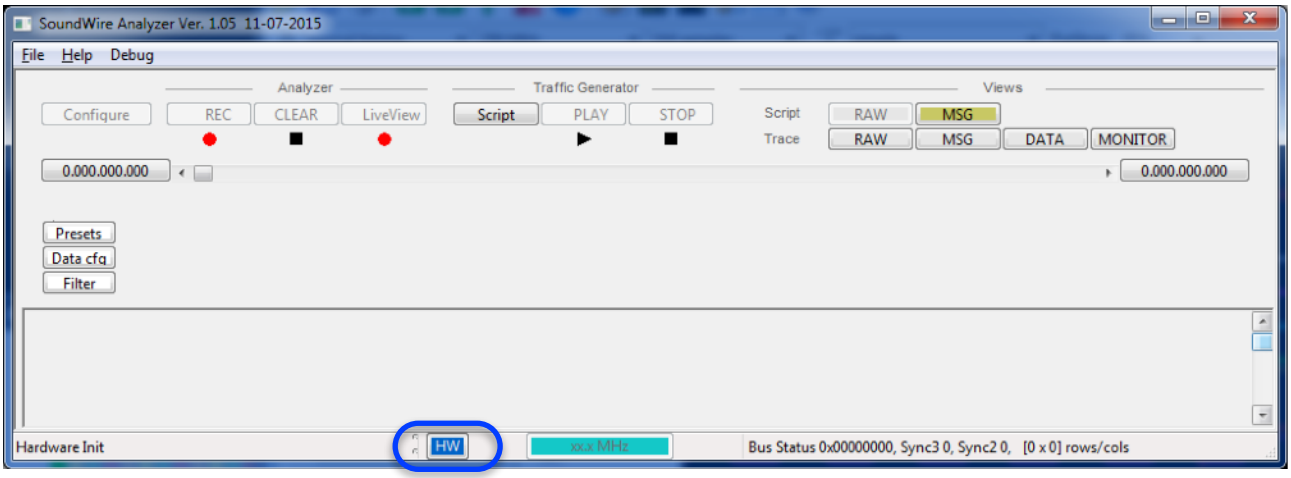
Make sure that the license key is plugged on a USB port of the host PC.
Launch the analyzer application.

As soon as the application is running, it will search for the hardware unit and configure it.
As long as the hardware unit has not been detected and configured by the PC, its display will show a standby message asking for PC connection.

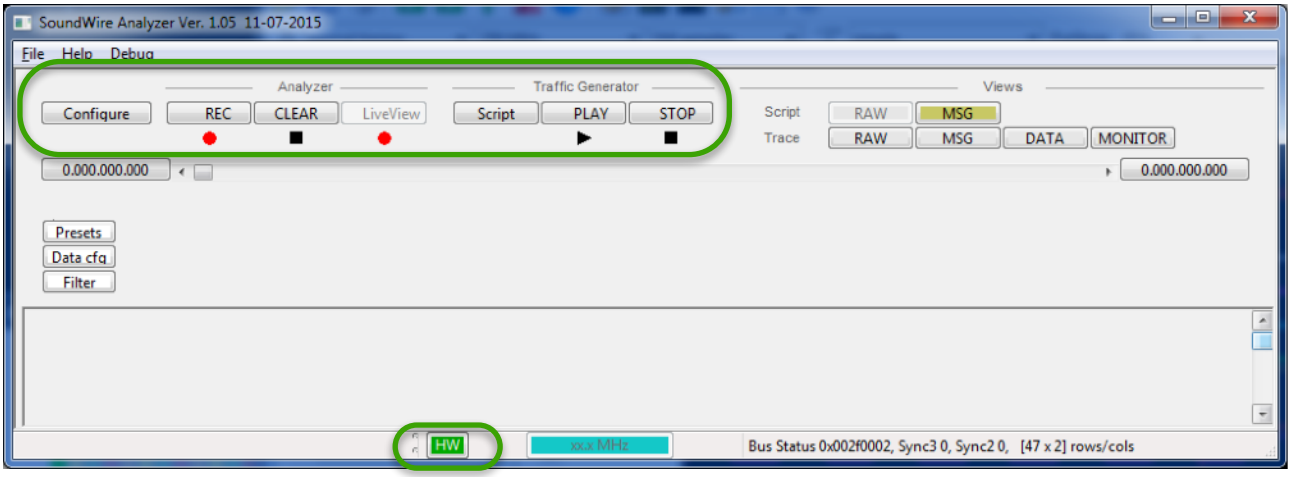
The HW status can be seen in the status bar at the bottom of the window. The hardware functions (like record and play) are greyed out if the hardware is not available.



HW not present or non configured



HW detected and being configured

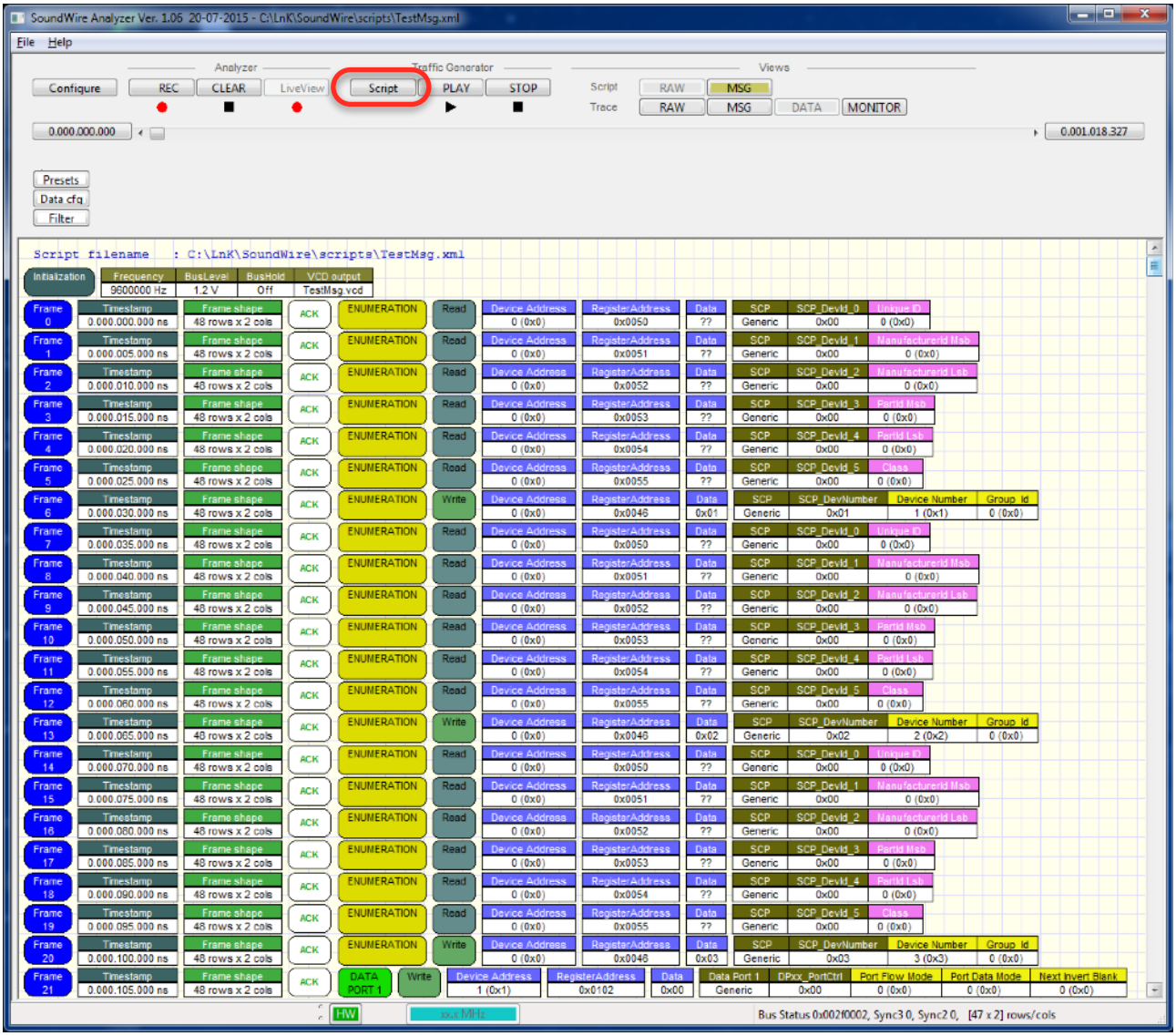


HW detected and configured

2.3. Load a script in the traffic generator

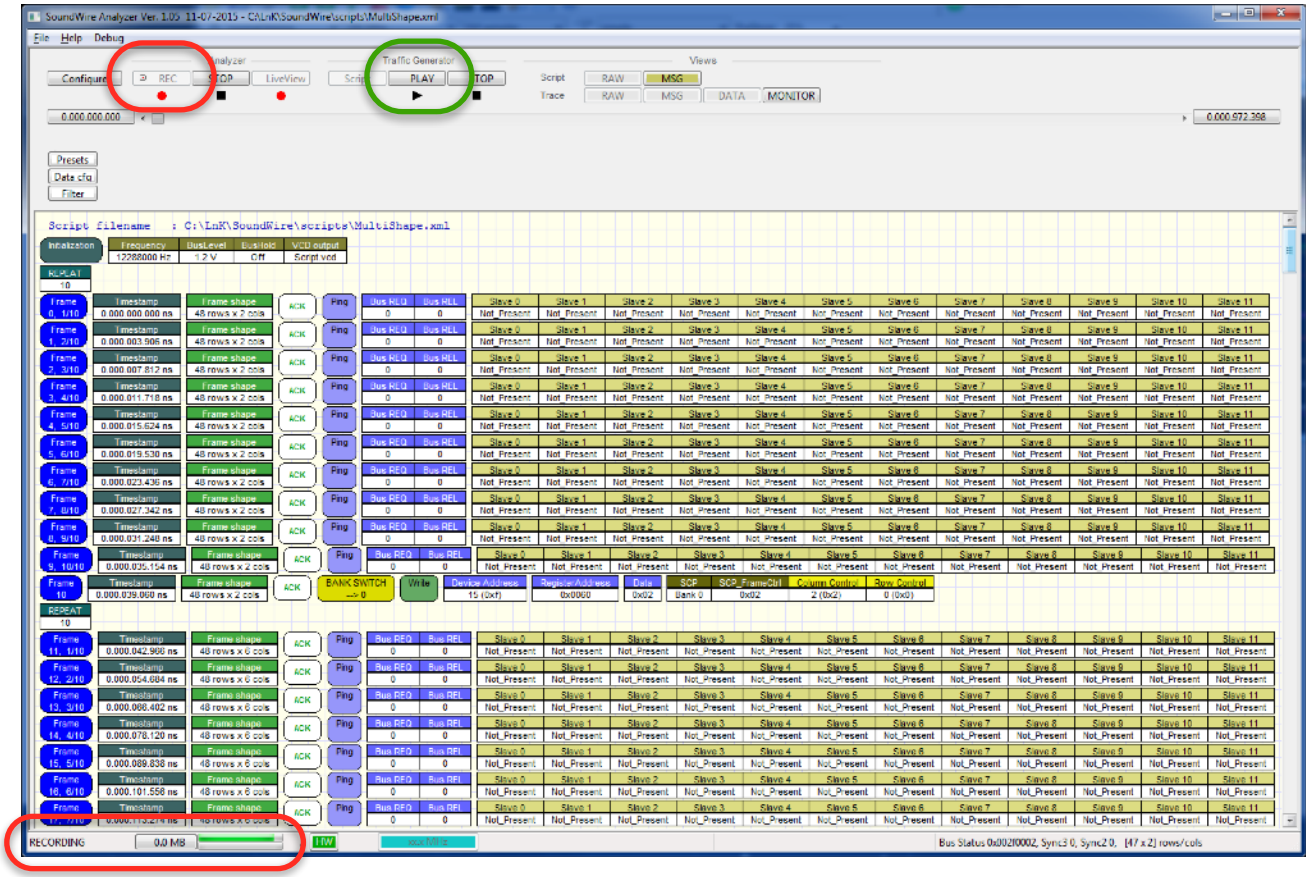
There are 2 ways to load a script in the traffic generator:

- Load an XML script from the traffic generator itself (though File menu or by pressing the Script button)
- Push it directly from the script editor (use CTRL+T or press the button **Send to TG** in the Finalize window).



The script content is shown in the main analyzer window.

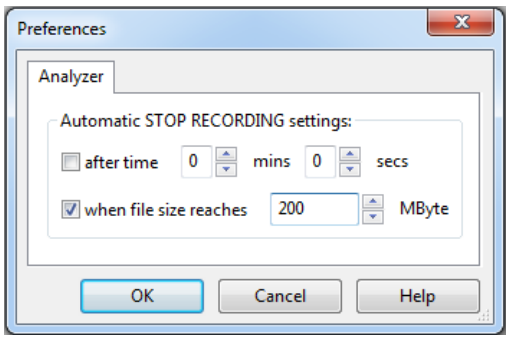
2.4. Play and record a script

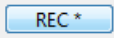


First press the **REC** button. Once pressed, it is greyed out. The analyzer is waiting for any clock activity on SoundWire to start the recording process. It's possible to stop the recording at any moment by pressing the **STOP** button besides the **REC** button. The amount of recorded data is shown in the status bar, on the bottom left side of the window. The maximum record size is now limited to 500 MB to prevent internal database files exceeding 4GB.
Then, press the **PLAY** button of the Traffic Generator to stream out the script. Once the script has been executed, press the **STOP** button of the analyzer to start the decoding of the recorded stream.

2.4.1. Recording options

File -> Preferences



Recording can be limited by defining a maximum time period or by a certain maximum file length. This is useful when recording is started due to a trigger event so only the relevant trace is being recorded and avoiding unnecessary long processing time and large files.
The REC button will have a '*' added 

when a limiting option is enabled.

2.4.2. Full recording mode

Full Recording is capturing all the bits from the bus and is able to reconstruct the complete trace and decoding and extracting all audio data.
This mode is consuming a lot of disk space and decoding time but gives the most detail.
While recording, the Live View is combined, so all relevant messages are shown on the screen while happening on the bus.

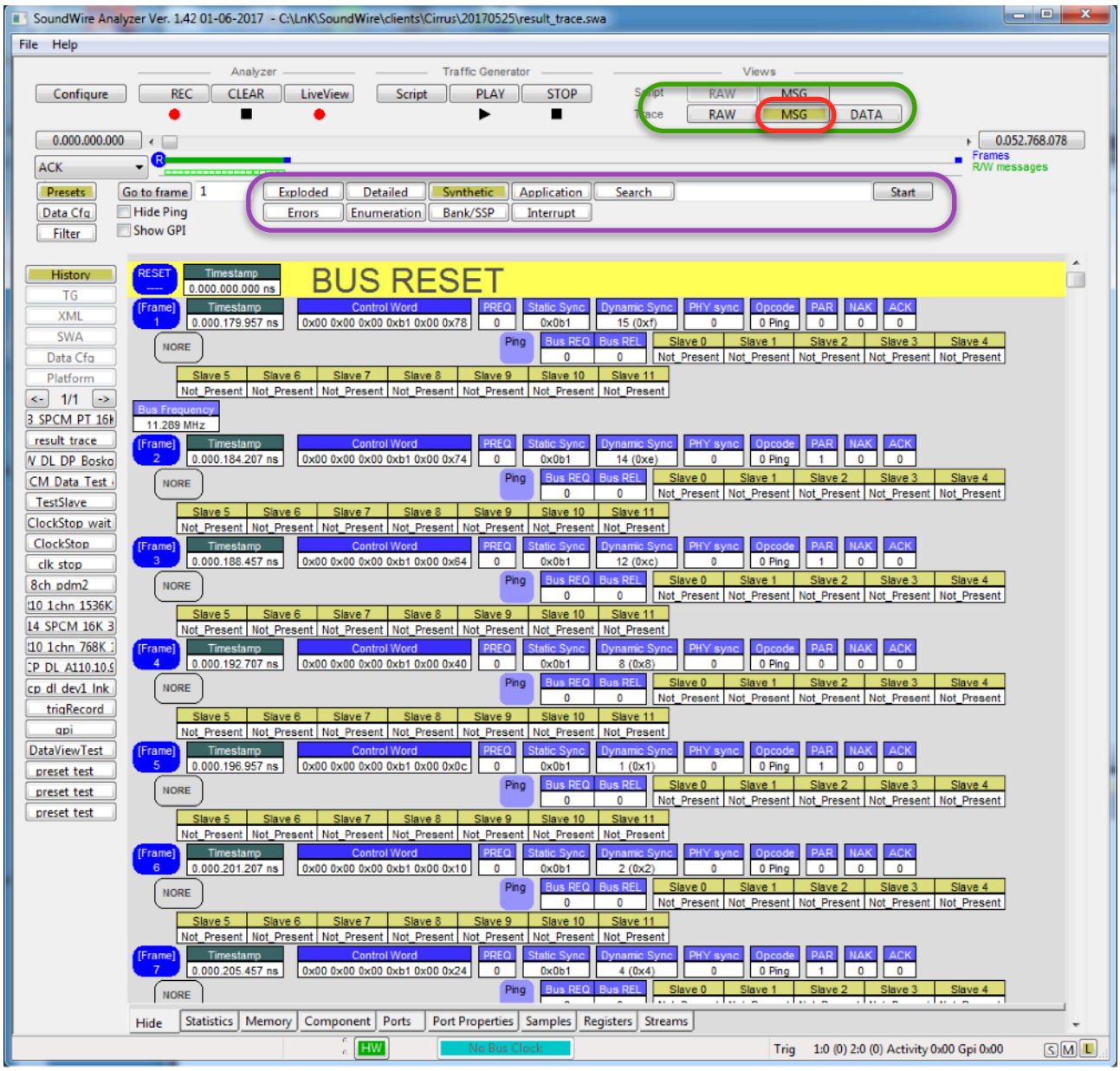
2.4.3. Live View

Live view is a monitor of all relevant messages captured from the bus. This mode is not capturing all the data bits from the bus thus it is not possible to reconstruct any audio data.
But the capturing of the messages is allowing to build up the configuration and show all detected data port and device configurations.

3. Stream analysis

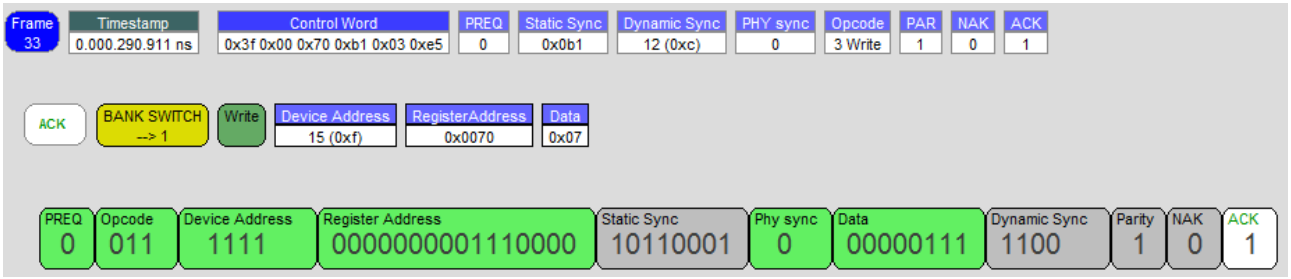
The protocol analyzer software offers various levels of reading of the captured SoundWire bit stream.

3.1.1. Message View

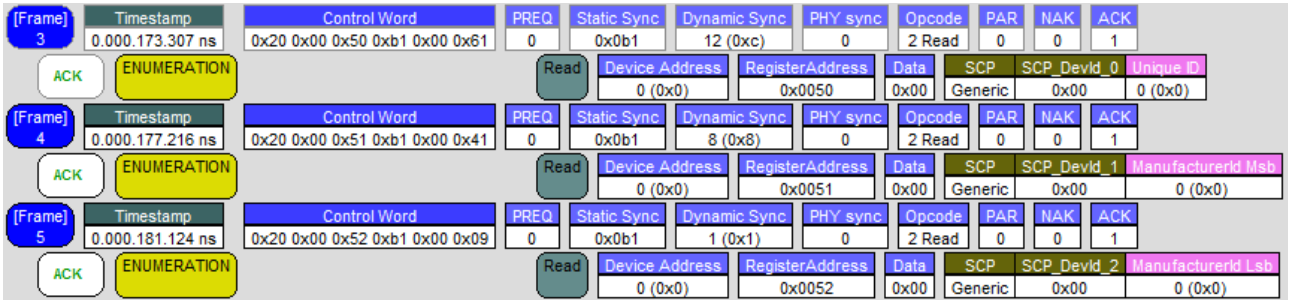


The Message View has multiple levels of analysis:

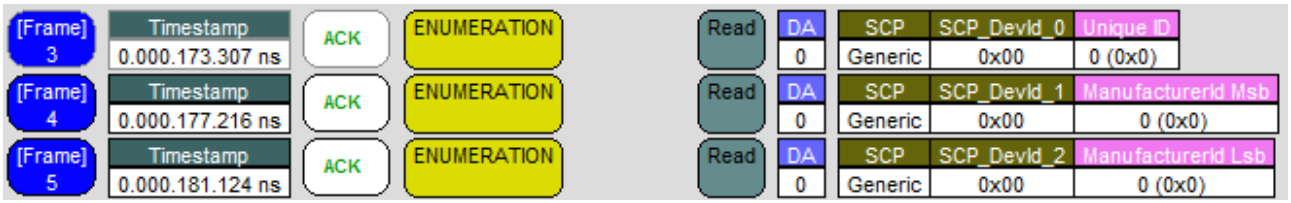
- **Exploded**. Each message is decoded at the bit level and displayed as such.



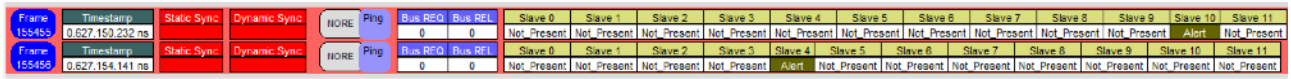
- **Synthetic**. The messages are decoded and shown in a list.



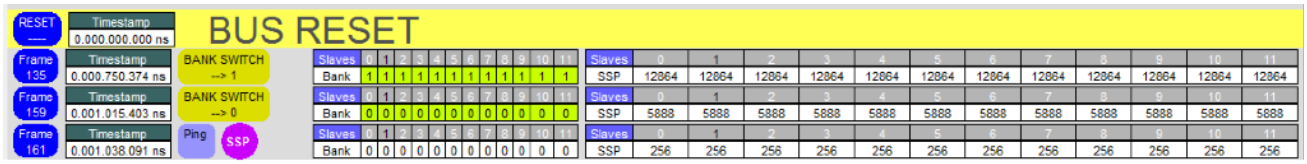
- **Application**. The frame information is hidden and messages only show the relevant information to understand the message flow.



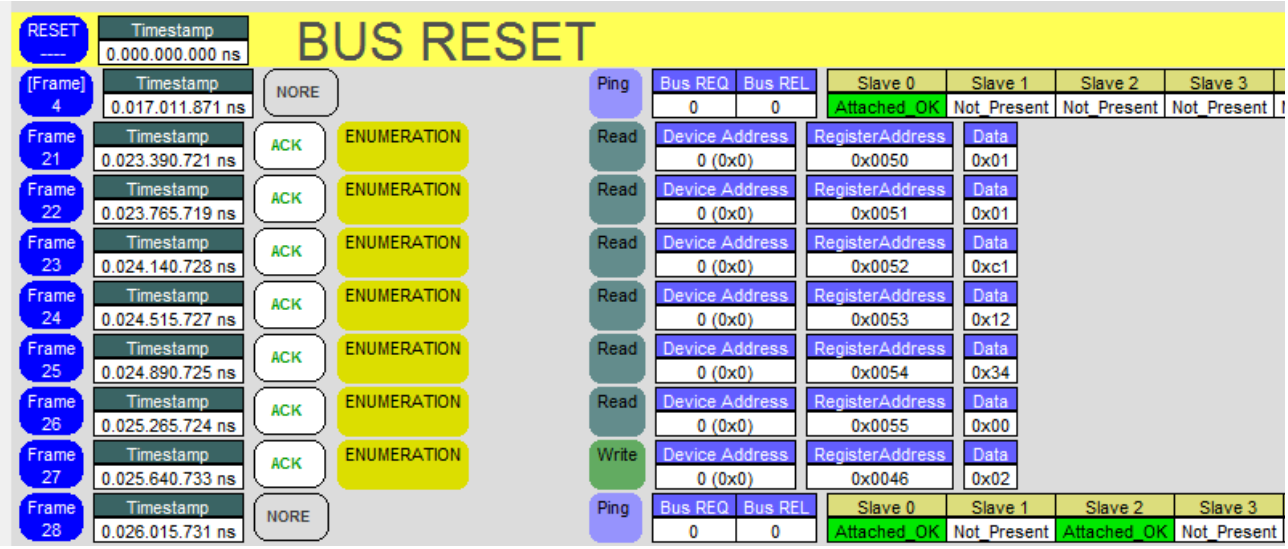
- **Errors**. All frames that are obtaining errors are listed here. That is easy to navigate to a certain error and then switch back to a more generic view such as Application view.



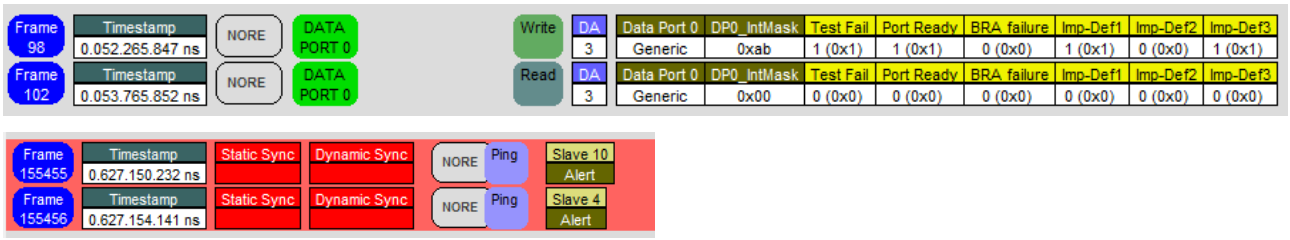
- **Enumeration**. Here all enumeration related events are shown.



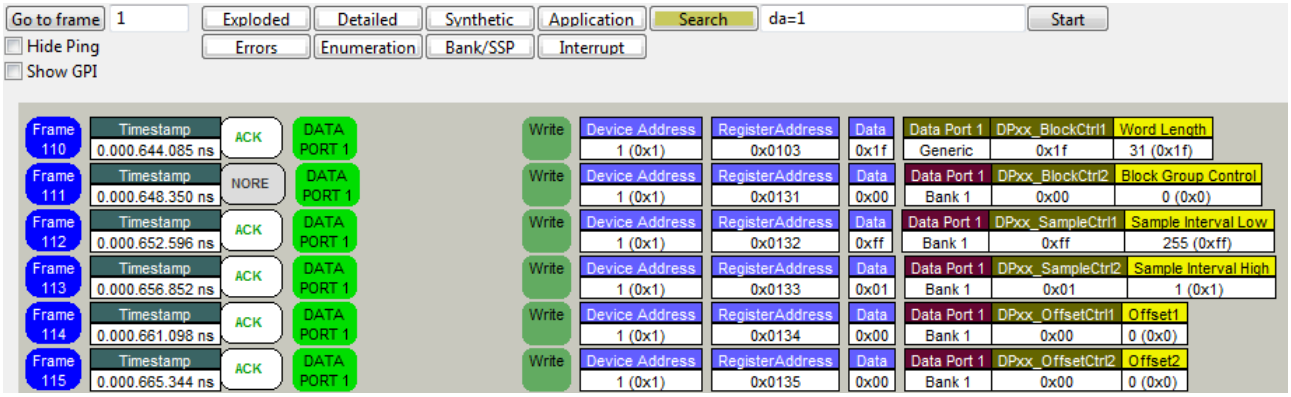
- **Bank/SSP**. Only Bank switching and SSP related events are shown.



- **Interrupt**. Only interrupt related events are shown.

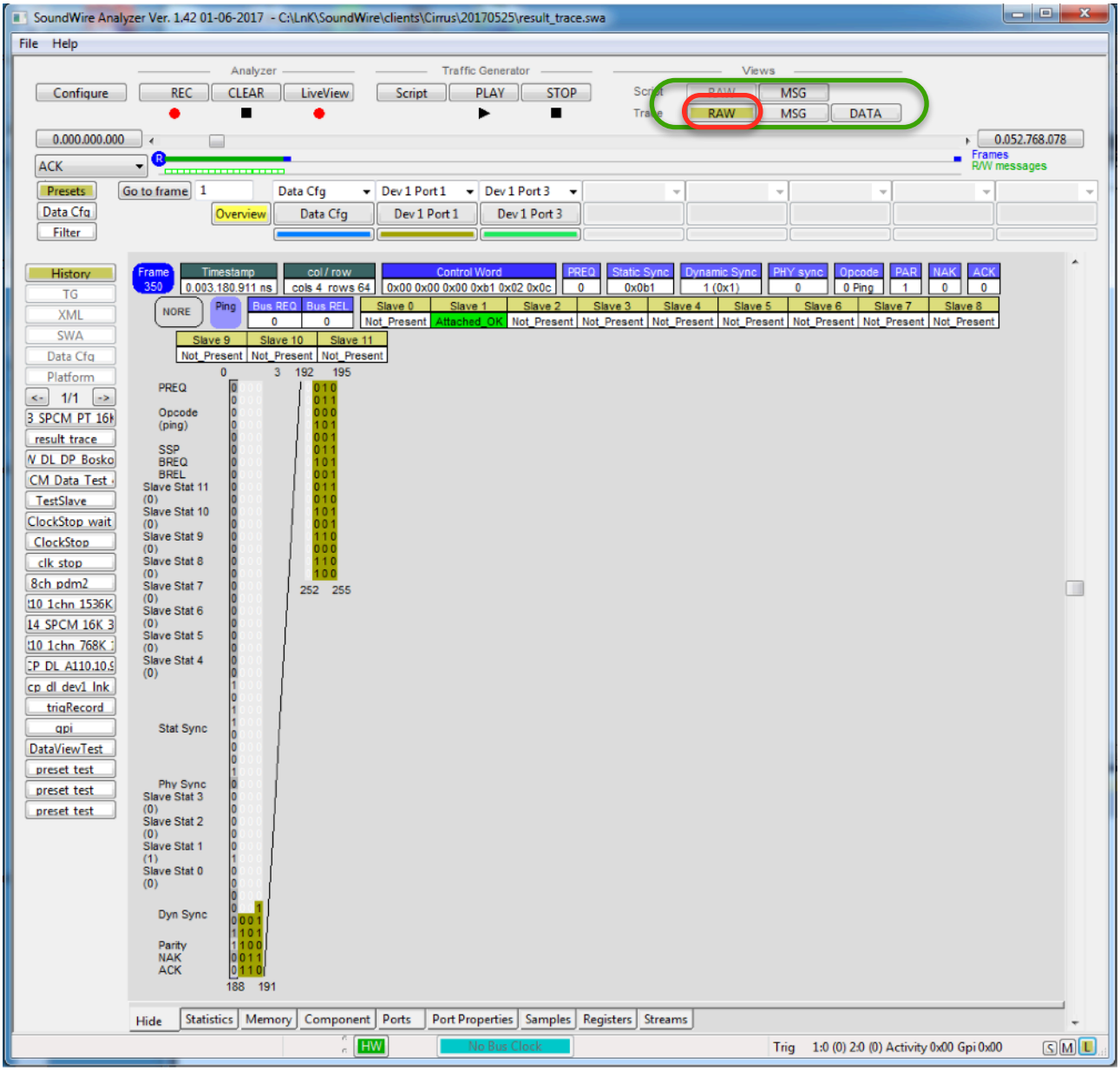


- **Search**. This is a text based search with the following keywords or combinations:
  write, read, ping, da=1, da=0x1, ra=304, ra=0x0130, data=3, data=0x03, ack=1, nak=0, bank, ssp, slavestatus=changed, preq, reset, error, bus_reset



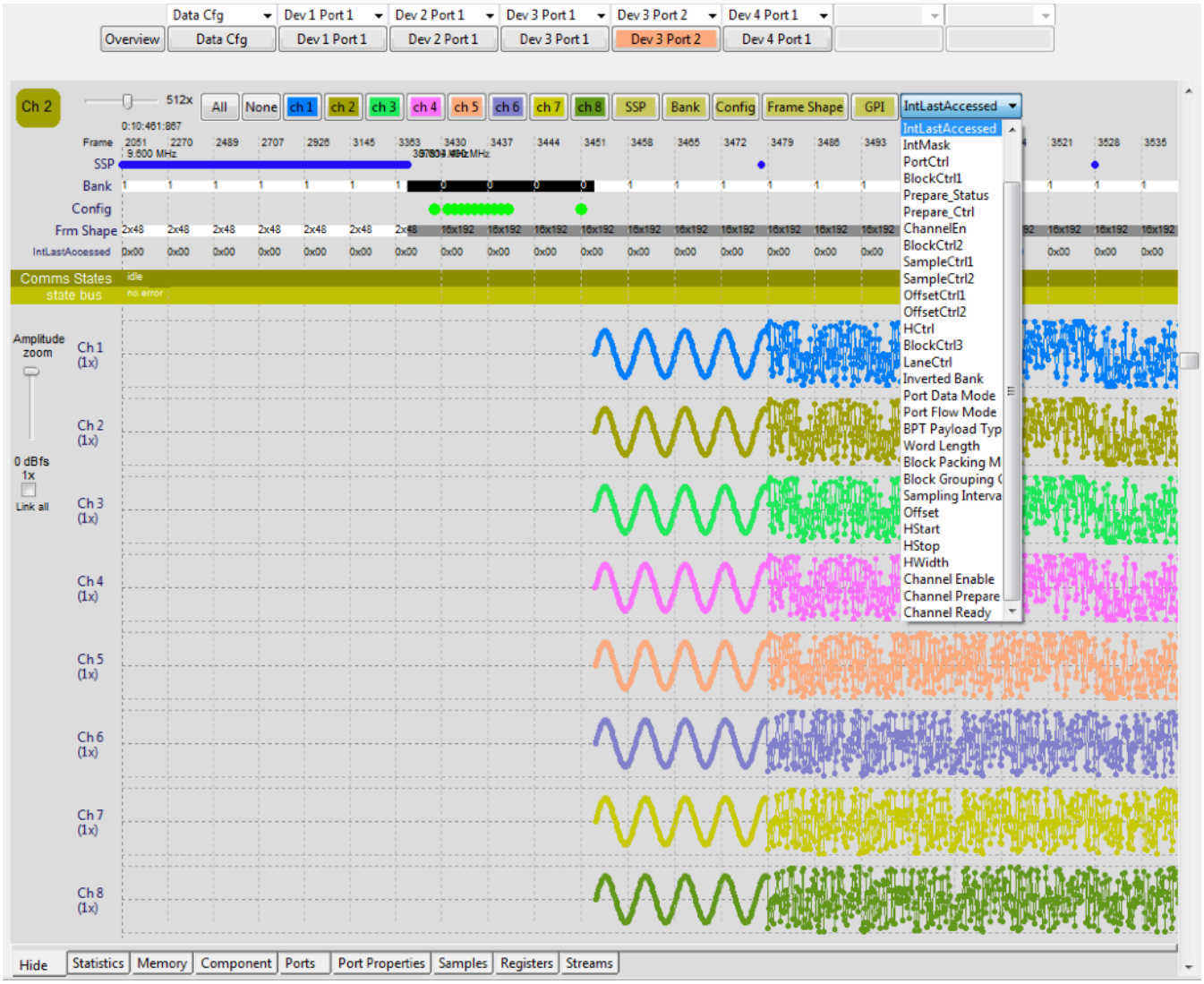
3.1.2. RAW View

The Raw View shows the frame shape and the content of every BitSlot. The BitSlots belonging to data stream are highlighted with different colors. The frame information and Control Word are shown for every frame. The unused bit slots are written in white. The configured bit slot from data channels are written in black with a color background representing there port. The first column contains the control word. If bit slots with a '1' value are detected in unconfigured data space they are coloured red to flag an error.

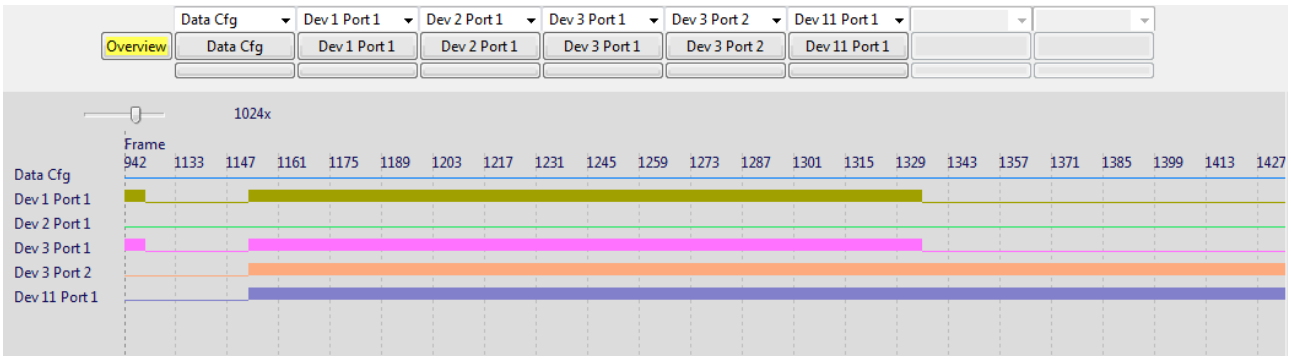


3.1.3. DATA View

The main purpose of the DATA View to to show the configuration and content of the different data streams active on the SoundWire bus at a given moment in time.



Up to 7 configured data ports are mapped onto the data port selection buttons together with a user “Data Config” button. If there are more than 7 configured data ports they are selectable through the listbox above every port button.

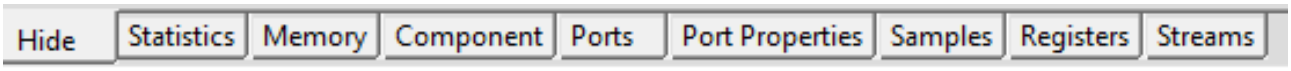


Display options:

- Time zoom factor: 1x - 32768x
- Channel selection: All, None, all available channels
- SSP: Stream Synchronisation Point indicated by a blue dot
- Bank: the current selected Bank alternating background of black and white with the value of the bank
- Config: A yellow dot show a write operation to the SCP or Data port registers
- Frame Shape: Shows the frame shape on an alternating background color. ex 2x48
- GPI: General Purpose Inputs are shows as defined in the GPI config. As 1 line or as a bus.
- A system or data port register values are displayed over the time line

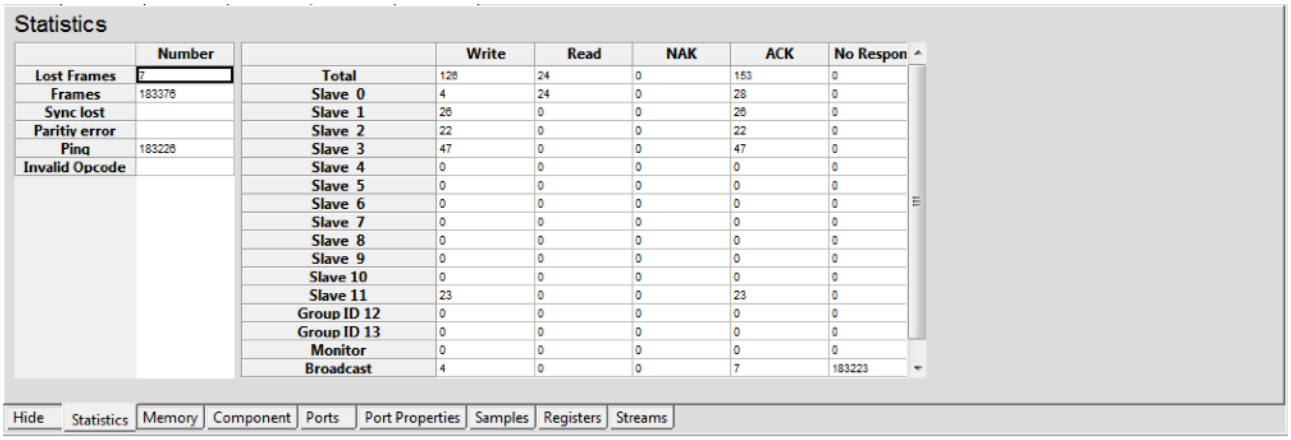
3.1.4. Info notebook

There is a Info notebook at the bottom of the views. Default it is hidden.



1. Statistics

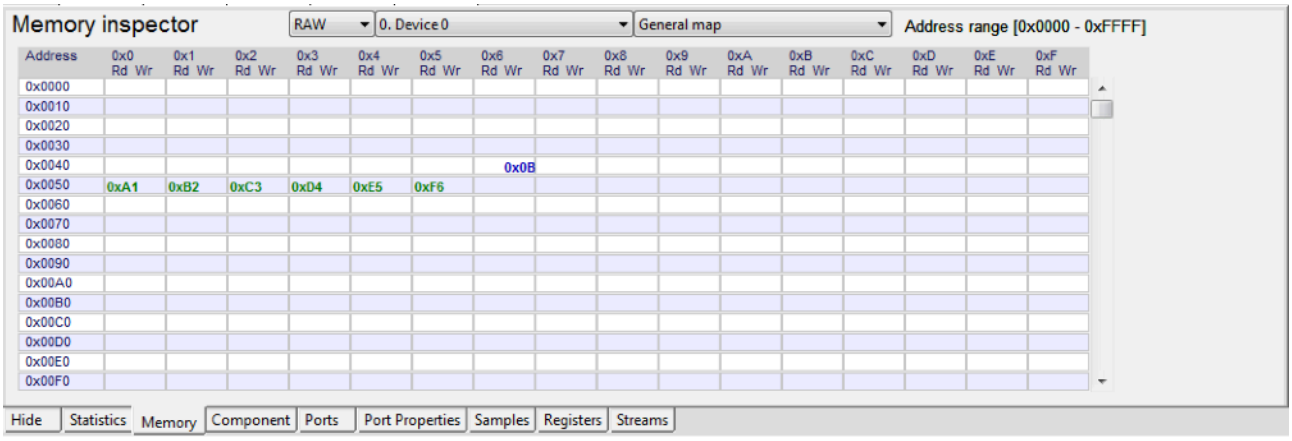
This page shows an overview of message and bus events as seen at the end of the recording.



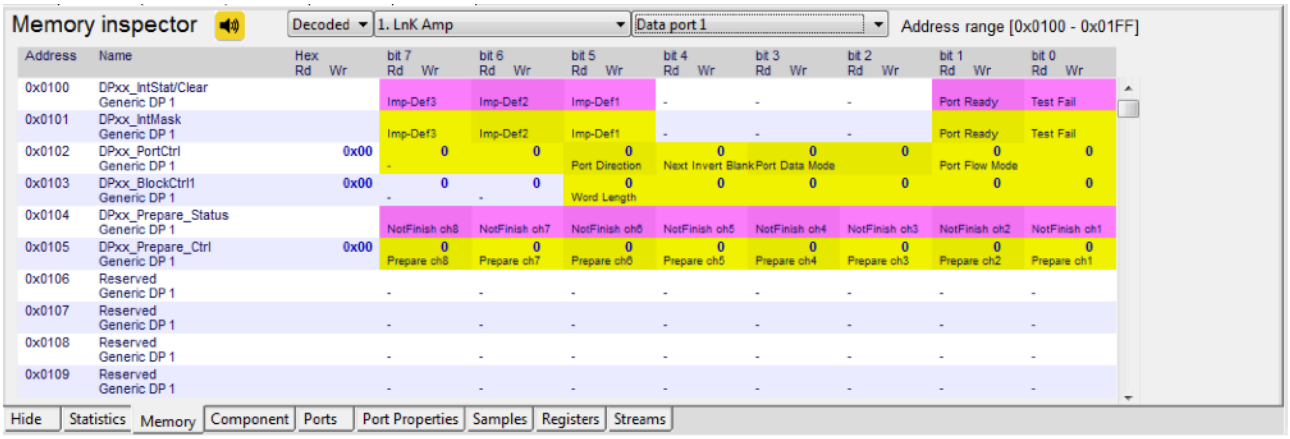
2. Memory Inspector

The memory inspector has two modes. The RAW mode which is showing the register values in Hex for the last read in green and last write operation in blue separately. The last action is drawn in bold. Note that this values are taken out of the read and write messages on he bus which is not a guarantee that the register is still containing the indicated values.
A general memory map shows the complete 64K range and also the different data port and system area are selectable together with eventual define regions of specific devices. See component editor of script builder,

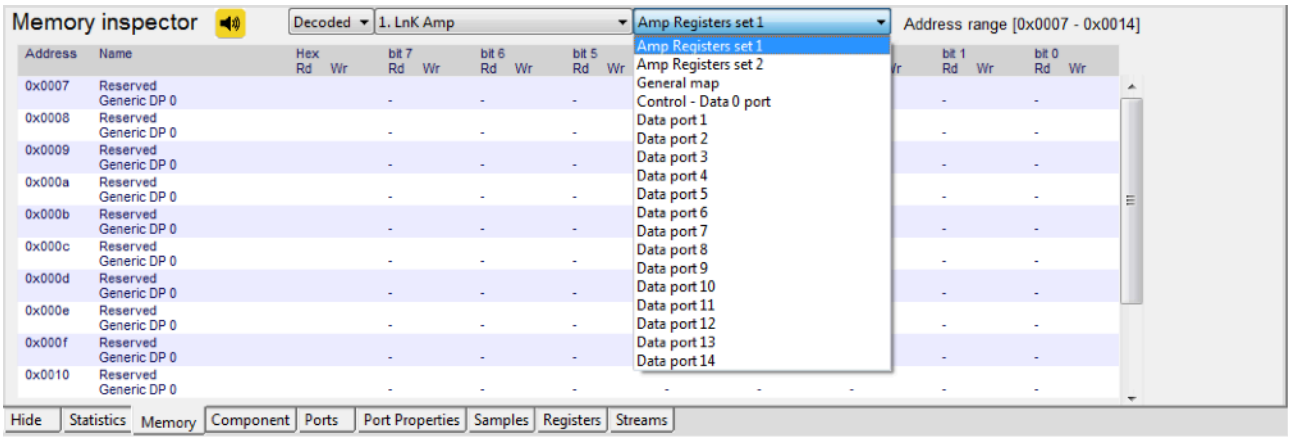
RAW mode:



Decoded mode indicates the name of the register and has all the bit fields explained as written in the SoundWire specification so it is clear what was written to or read from that register.

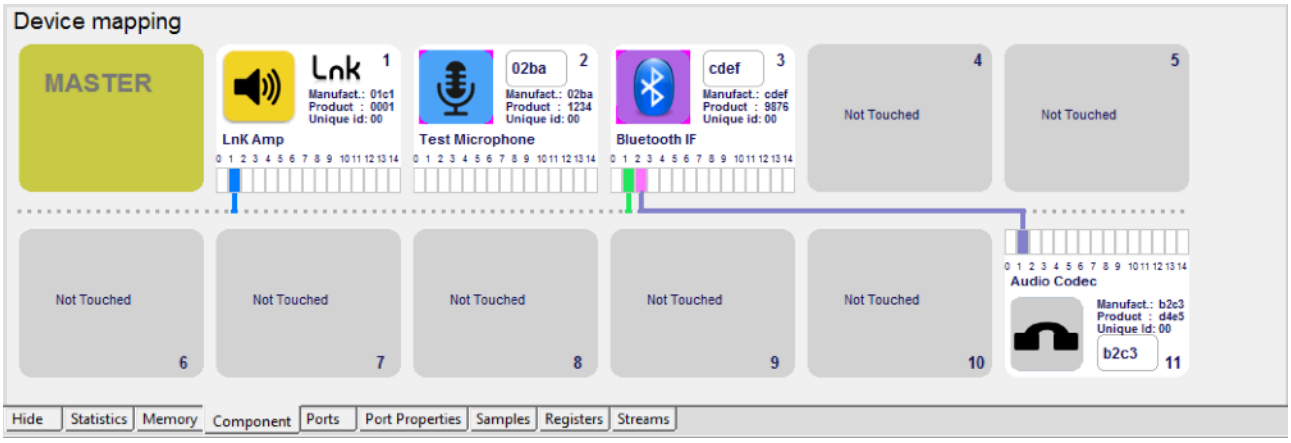


When A component has defined in the component library (via script builder or xml) then specific regions are added to the choice list.



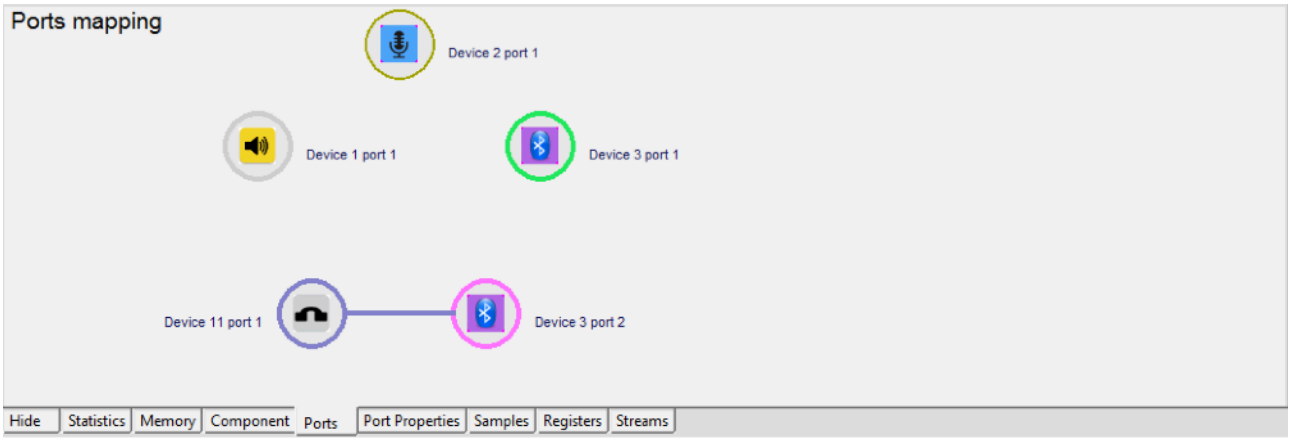
3. Device Mapping

The software can detect the different devices on the bus and displays them with the enumeration information and data port use. Enabled data ports are indicated and if data ports have the same configuration, they will be connected together. This option is very handy during the live view and so a device map with data port activity will be up to date on what is happening on the bus.
If a full recording has been done or a *.swa or an *.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor.



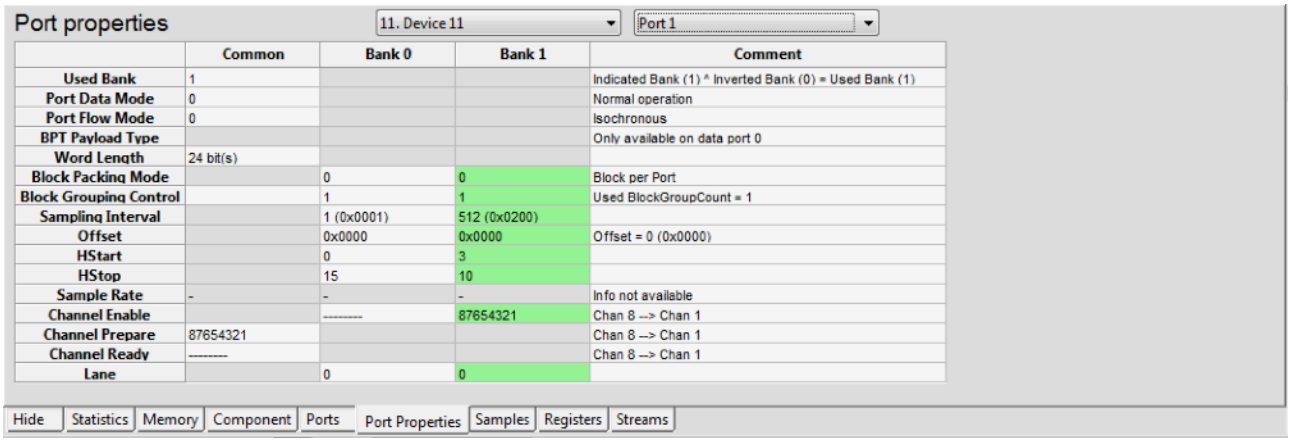
4. Ports Mapping

In this page are all the detected data ports. If the data port is not enabled it is displayed with a thin circle and when it is enabled, it is indicated by a thick circle. If data ports have the same configuration they are drawn as connected.If a full recording has been done or a *.swa or an *.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor.When the analyser is in live view, the page is showing the current situation of the bus.



5. Port Properties

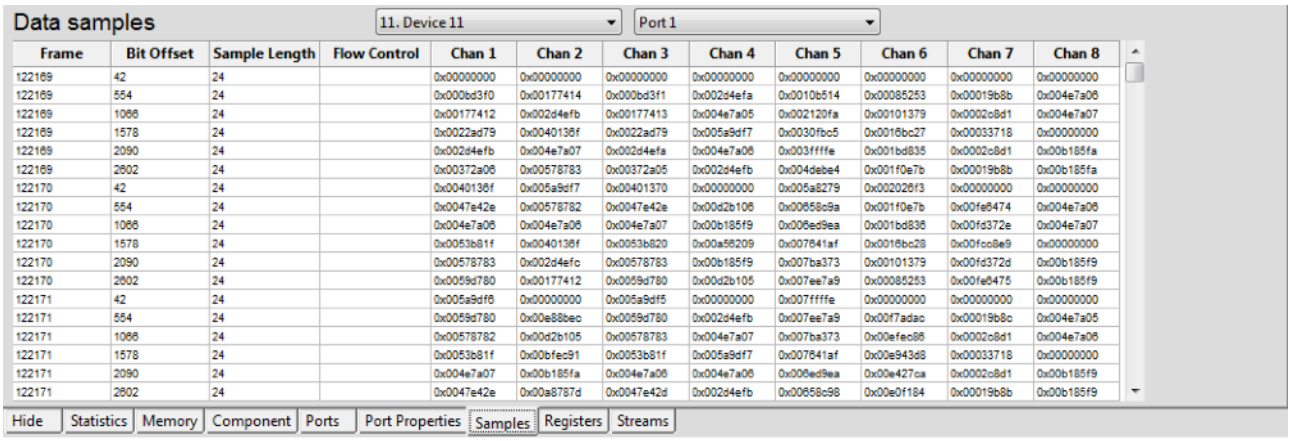
In this page the data port configuration parameters are shown. The active bank is high lighted. If a full recording has been done or a *.swa or *.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor. When the analyzer is in live view, the page is showing the current situation of the bus.



	Common	Bank 0	Bank 1	Comment
Used Bank	1			Indicated Bank (1) ^ Inverted Bank (0) = Used Bank (1)
Port Data Mode	0			Normal operation
Port Flow Mode	0			Isochronous
BPT Payload Type				Only available on data port 0
Word Length	24 bit(s)			
Block Packing Mode		0	0	Block per Port
Block Grouping Control		1	1	Used BlockGroupCount = 1
Sampling Interval		1 (0x0001)	512 (0x0200)	
Offset		0x0000	0x0000	Offset = 0 (0x0000)
HStart		0	3	
HStop		15	10	
Sample Rate	-	-	-	Info not available
Channel Enable		--------	87654321	Chan 8 --> Chan 1
Channel Prepare	87654321			Chan 8 --> Chan 1
Channel Ready	--------			Chan 8 --> Chan 1
Lane		0	0	

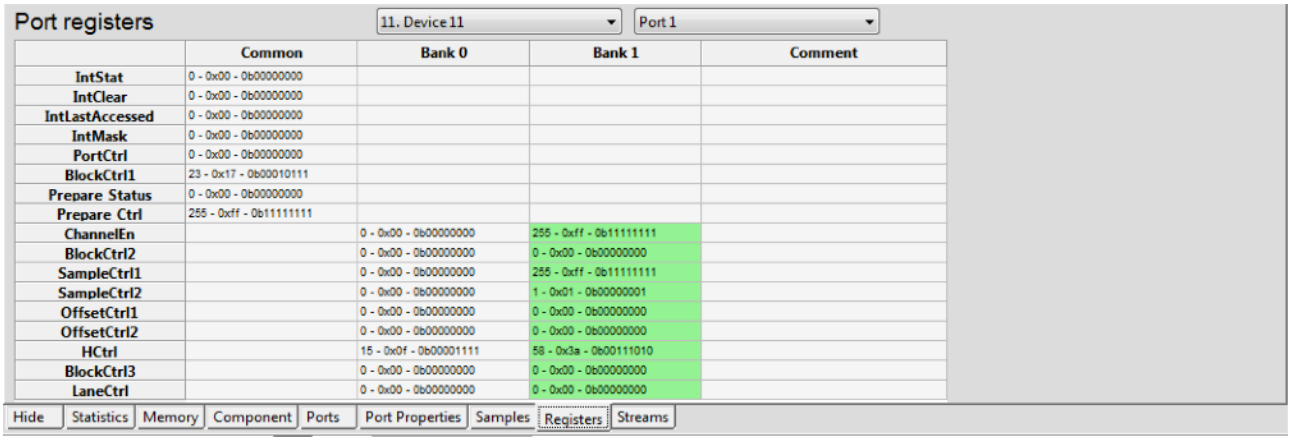
6. Data Samples

This page is only valid when loading a *.swa or *.fvf file or when done a full recording.



7. Port Registers

In this page the data port registers are shown in decimal, hexadecimal and binary. The active bank is high lighted.
If a full recording has been done or a *.swa or *.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor. When the analyzer is in live view, the page is showing the current situation of the bus.



8. Stream Mapping

The Stream Mapping table shows all the data ports for all the slave devices. If a data port is used, it is coloured. When it is active, it wil contain a stream number. All the data ports that have the same number are connected.
If a full recording has been done or a *.swa or *.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor. When the analyzer is in live view, the page is showing the current situation of the bus.