



# SoundWire Analyzer

## User Manual



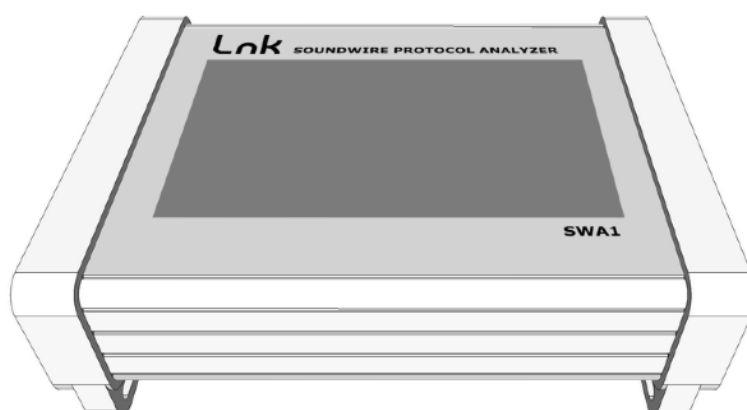
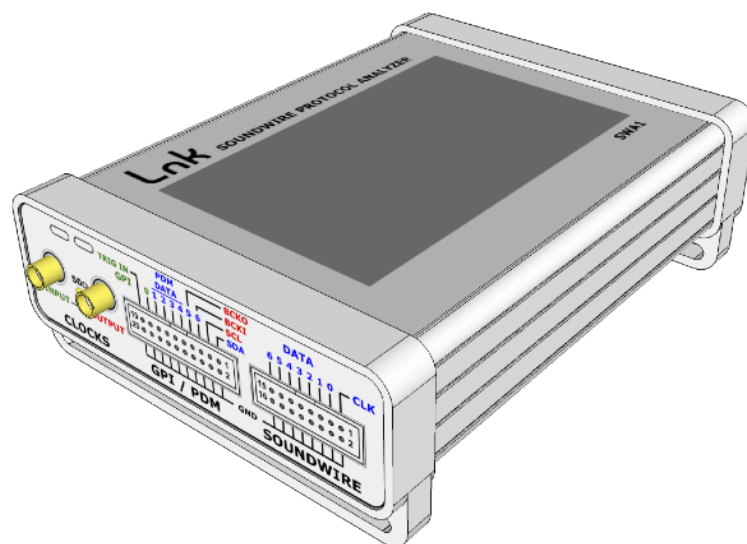
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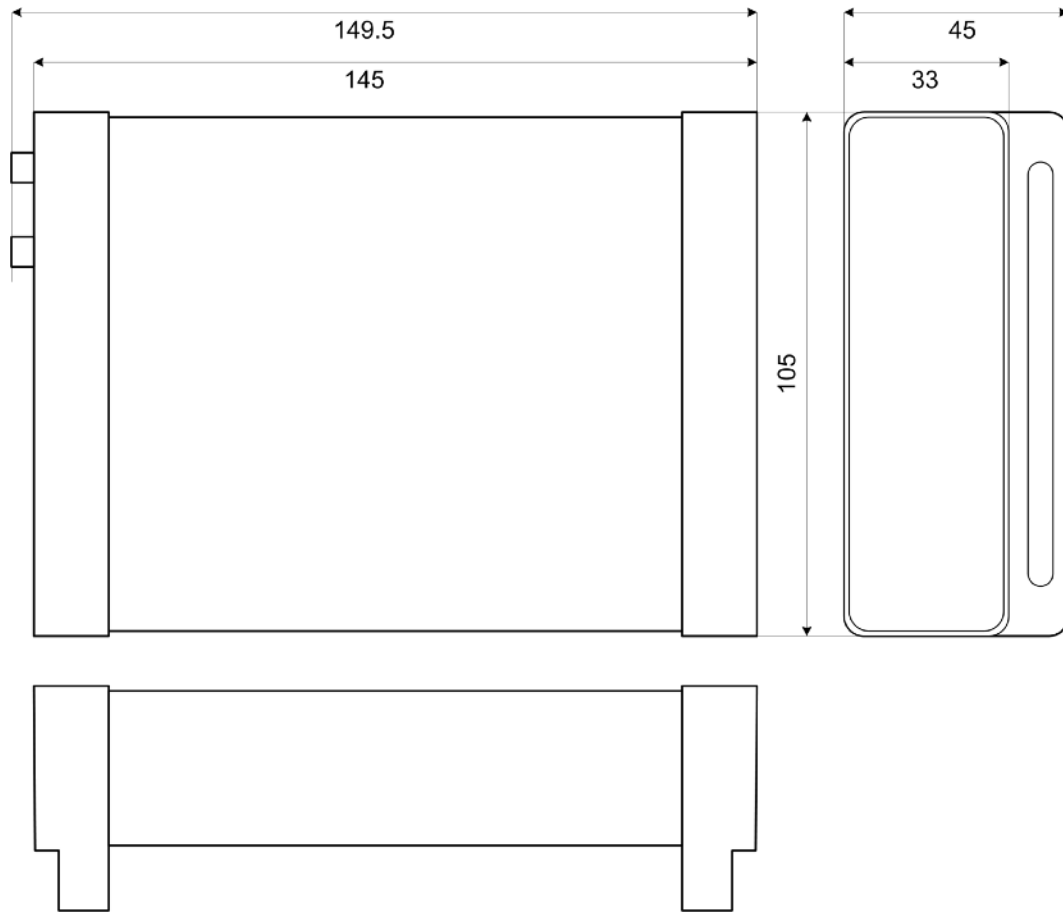
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## 1. HARDWARE SPECIFICATION



## 1.1. Hardware dimension



All dimensions are in millimetres.

Unit weight : 490 g.

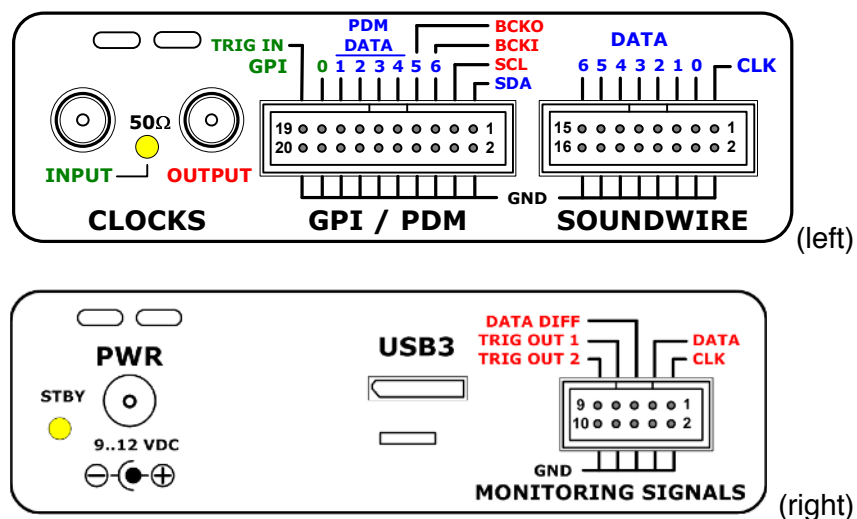
Body material: anodised aluminium.

## 1.2. User Interface

All the hardware controllable features are accessible through the 4.3" colour touch screen of the unit.

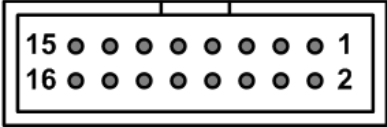
## 1.3. Connectivity

The unit has multiple connectors located on the left side and on the right side.



### 1.3.1. SoundWire bus connector

The SoundWire signals (clock and data) are available on a boxed IDC 16 pin header connector with a regular pitch of 2.54 mm (0.1"). The bottom pins are all connected to ground.

Pin	Signal	Direction	
1	Clock	Input & output	
3	Data Line 0 (main)	Input & output	
5	Data Line 1	Input & output	
7	Data Line 2	Input & output	
9	Data Line 3	Input & output	
11	Data Line 4	Input & output	
13	Data Line 5	Input & output	
15	Data Line 6	Input & output	
2..16	Ground		

The data line bus keepers cannot be controlled individually. Either all ON or all OFF.

Electrical Parameter	Min	Nominal	Max	Units	Remarks
SoundWire signaling level	0.9	1.8	3.2	V	Programmable by steps of 50 mV
Bus Keeper impedance	6950		1M	Ohms	Bus keeper can be deactivated
Output impedance	15			Ohms	
Input impedance		1M		Ohms	When Bus Hold is disabled

### 1.3.2. Multi-purpose connector

The signals (clock and data) are available on a boxed IDC 20 pin header connector with a regular pitch of 2.54 mm (0.1"). The bottom pins are all connected to ground.

This connector serves multiple purposes. It features an I2C interface that can either acts as a slave or as a master (not implemented yet). There is a dedicated trigger input pin. Six of the seven general purpose input pins can be reassigned to a multichannel PDM input & output interface or a multichannel PCM input or output.

Electrical Parameter	Min	Nominal	Max	Units	Remarks
GPI & I2C signaling level	0.9		3.2	V	Programmable by steps of 50 mV
Output impedance	47			Ohms	
Input impedance		47k		Ohms	

FUNCTION								
Pin	GPI		PDM 8 CH IN		PDM 4 IN / 4 OUT		PDM 8 CH OUT	
1	I2C_SDA	I/O	I2C_SDA	I/O	I2C_SDA	I/O	I2C_SDA	I/O
3	I2C_SCL	I/O	I2C_SCL	I/O	I2C_SCL	I/O	I2C_SCL	I/O
5	GPI6	IN	PDM_BCKI	OUT	PDM_BCKI	OUT	PDM_BCKI	OUT
7	GPI5	IN	PDM_BCKO	OUT	PDM_BCKO	OUT	PDM_BCKO	OUT
9	GPI4	IN	PDM_DATA4	IN	PDM_DATA4	OUT	PDM_DATA4	OUT
11	GPI3	IN	PDM_DATA3	IN	PDM_DATA3	OUT	PDM_DATA3	OUT
13	GPI2	IN	PDM_DATA2	IN	PDM_DATA2	IN	PDM_DATA2	OUT
15	GPI1	IN	PDM_DATA1	IN	PDM_DATA1	IN	PDM_DATA1	OUT
17	GPI0	IN	GPI0	IN	GPI0	IN	GPI0	IN
19	TRIG IN	IN	TRIG IN	IN	TRIG IN	IN	TRIG IN	IN
2..20	Ground							

FUNCTION				
Pin	PCM 8 CH IN		PCM 8 CH OUT	
1	I2C_SDA	I/O	I2C_SDA	I/O
3	I2C_SCL	I/O	I2C_SCL	I/O
5	PCM_BCLK	OUT	PCM_BCLK	OUT
7	PCM_LRCLK	OUT	PCM_LRCLK	OUT
9	PCM_DATA4	IN	PCM_DATA4	OUT
11	PCM_DATA3	IN	PCM_DATA3	OUT
13	PCM_DATA2	IN	PCM_DATA2	OUT
15	PCM_DATA1	IN	PCM_DATA1	OUT
17	GPI0	IN	GPI0	IN
19	TRIG IN	IN	TRIG IN	IN
2..20	Ground			

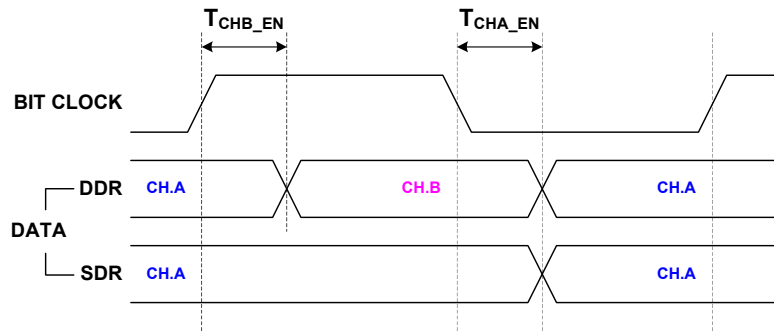
### 1.3.2.1. GPI operation

The GPI pin logical levels are all sampled by the analyzer at the beginning of every frame. The captured value are shown in the analyzer traces.

### 1.3.2.2. Serial Audio Interface

The interface is always a clock **master** because clocks are either directly derived from the SoundWire bus clock or generated from an external audio master clock. The Serial Audio Interface supports PDM and PCM streaming on up to 4 data lines.

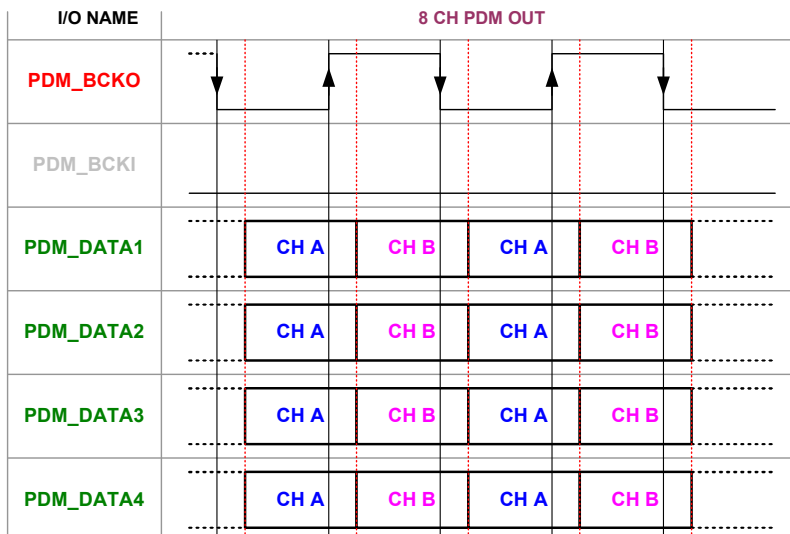
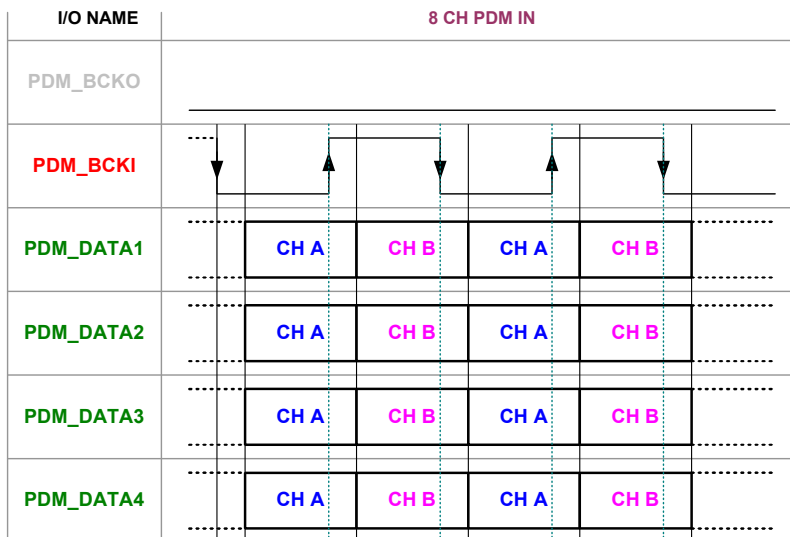




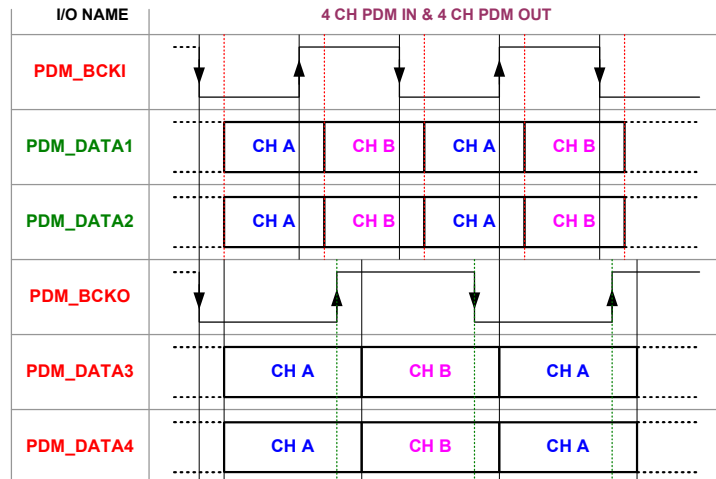
The interface can operate in a single data rate mode (PDM and PCM) or in dual data rate mode (PDM only).

In single data rate mode (SDR), the data is set after the falling edge of the bit clock. The delay between the clock falling edge and the data edge ( $T_{CHA\_EN}$ ) is equal to **13.6 ns**. The data line is sampled on the clock rising edge.

In dual data rate mode (DDR), the data is set after every clock edge (falling or rising). The delay between the clock falling edge and the data edge ( $T_{CHA\_EN}$ ) is equal to **13.6 ns**. The delay between the clock rising edge and the data edge ( $T_{CHB\_EN}$ ) is equal to **12.5 ns**. The data line is sampled on the every clock edge.



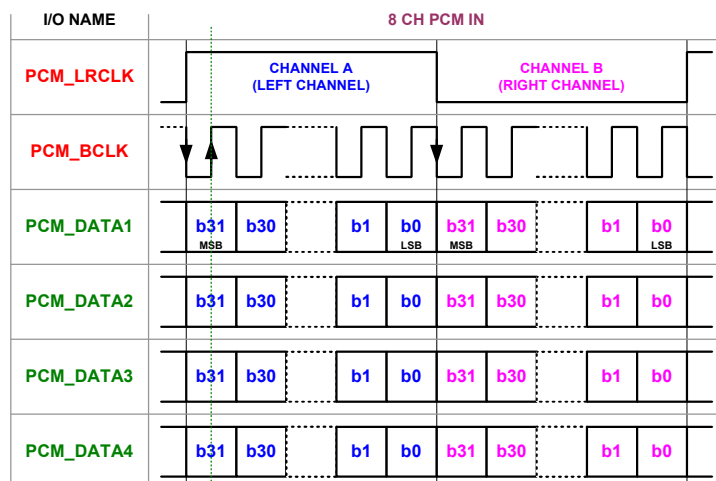
When the Serial Audio Interface is configured to allow both PDM input and output streams, the two bit clocks are totally independent (frequency, phase and time of activation).

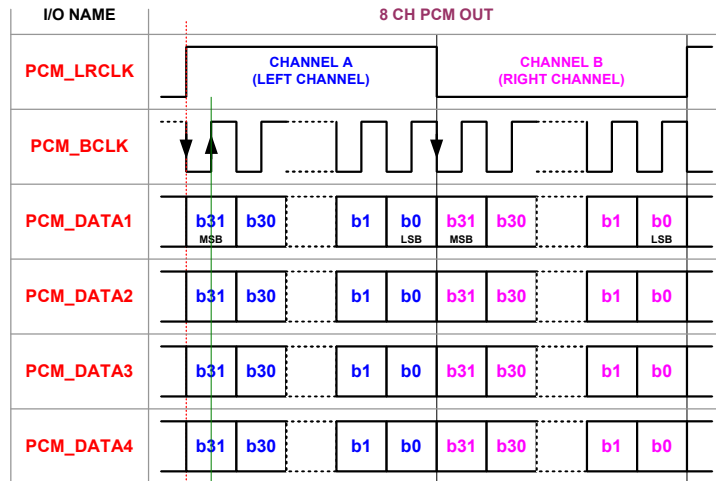


The PDM data paths have dedicated routers (one per data line) to increase the data handling flexibility of the interface. See the ScriptBuilder user manual for the configuration of these data routers.



When configured to operate in PCM mode, the interface generates a bit clock and a word clock. The word clock transition always happens on the falling edge of the bit clock. The bit clock is always 64 times greater than the word clock. The data are left aligned, MSB first and each frame channel is 32 bits long.





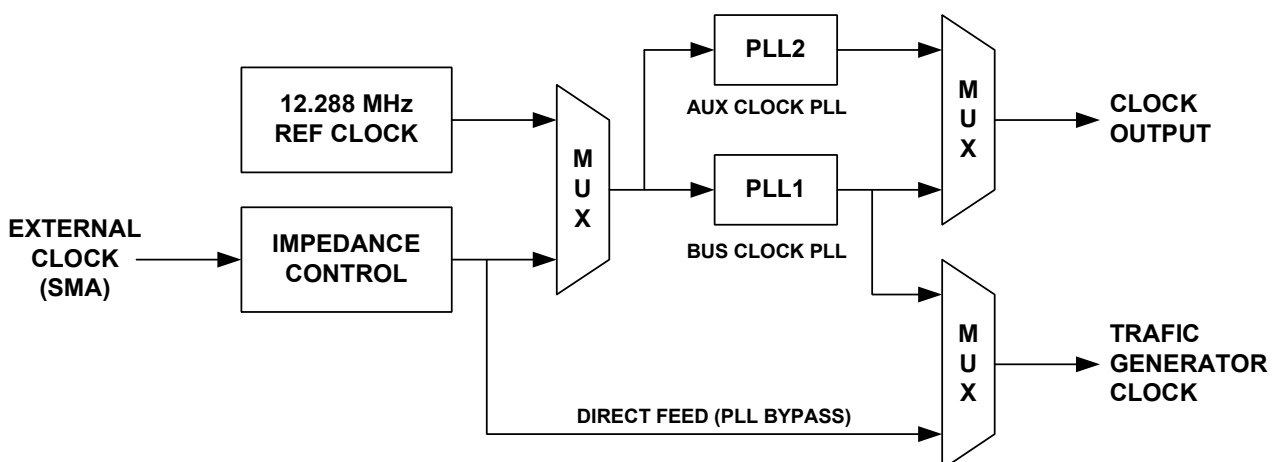
### 1.3.3. Clock input and output connectors

The unit can input an external clock to feed the SoundWire Traffic Generator. It can also output a configurable clock. The connectors are 50 Ohms SMA.

The input impedance is configurable and can be set to 50 Ohms or 1MOhms. The 50 Ohms state is indicated by a glowing yellow led close to the input connector. The clock signalling level is programmable (from 0.9V to 3.2V by steps of 50mv).

Electrical Parameter	Min	Nominal	Max	Units	Remarks
Clock signaling level	0.9		3.2	V	Programmable by steps of 50 mV
Output impedance		50		Ohms	
Input impedance	50		1M	Ohms	Programmable (50R or 1M)
Input frequency	1		50	MHz	When PLL are used
	0		26	MHz	When using direct feed

The unit has a flexible clock tree.



The traffic generator clock can be generated from a 12.288 MHz high purity oscillator or from an externally fed clock. The PLLs are actually bypassed when the desired frequencies can be derived from the reference clock by an integer divider. If this is not possible, the PLL is used.

It is possible to completely bypass the PLL chip to generate the traffic generator clock. It is therefore possible to proceed with direct injection of clock signals. This is especially interesting when jitter sensitivity tests of frequency variation tests must be performed.

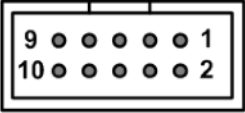
The external input clock can have an arbitrary value. The frequency is measured and the PLLs are configured to generate the desired target frequencies. However, it is always better to use common frequencies for audio and communication system. The unit software will compare the measured frequencies with known values and take the known values that are close (+/- 0.8%) to the measured frequency. This is done to reduce the risk of wrongly set target frequencies. If nothing matches, the PLL parameters will be computed with the measured input frequency value. When using the PLL, the lowest usable input frequency is 1 MHz.

**Note:** When using direct feed, the external clock frequency **must be twice** the desired SoundWire bus clock (SoundWire clock = 1/2 external clock).

The output clock is fed by one of the two PLL outputs. The Auxiliary clock frequency is manually programmable.

### 1.3.4. Monitoring Signals connector

The monitoring signals are available on a boxed IDC 10 pin header connector with a regular pitch of 2.54 mm (0.1"). The bottom pins are all connected to ground.

Pin	Signal	Direction	
1	Buffered SW clock	Out	
3	Buffered SW data	Out	
5	DATA DIFF	Out	
7	TRIG 1 OUT	Out	
9	TRIG 2 OUT	Out	
2..10	Ground		

The buffered SoundWire clock signal is a copy of the captured SoundWire clock. It enables scope probing without disturbing the bus. The buffered SoundWire data signal is a copy of one of the 7 SoundWire data lines. The selected line is control through a script command or directly via the PC application.

The Data Diff signal is high every time there is a difference between the transmitted data and the captured data. It indicates where the DUT is writing or if there is a bus clash condition.

The TRIG 1 and TRIG 2 outputs are used to flag specific events happening on the bus. The Trig Out signals are controlled directly by a script command (to spot a specific part of the script) or by an internal event decoder that flags specific events (especially in sniffer mode). The event filter engine is controlled via the PC application.

The monitoring signals use the same signaling level as the GPI/PDM connector.

### 1.3.5. USB3 connector

The unit needs to be connected to a PC for operation. It does not work as a stand-alone piece of equipment. A USB3 port is required on the PC to properly operate the unit. No power is drawn from the USB3 port. The unit is self powered.

### 1.3.6. Power supply connector

The unit needs an external supply to operate. The typical supply voltage is 9V. The power consumption depends on many parameters. At a minimum, the unit will consume 1.5 W. If the display is set to maximum brightness and the FPGA is loaded with an IP running a maximum of gates at full speed, the power consumption can reach 5 W.

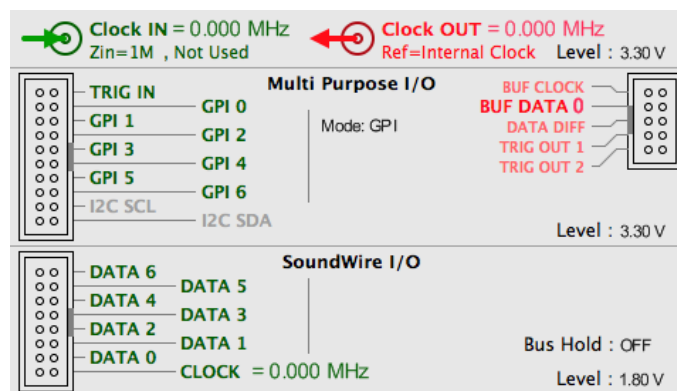
## 1.4. Hardware Operation

Connect the hardware unit to a USB3 port.

Power on the unit **before** launching the Protocol Analyzer software.

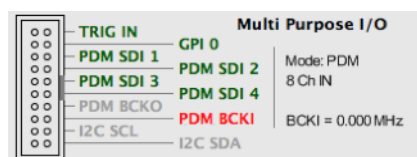
While the unit is waiting for the PC activation, the display will show a standby message asking for PC connection.

Once the Protocol Analyzer software has detected and configured the hardware, the display will show the main page, providing information about the system configuration and the various connector pin functions.

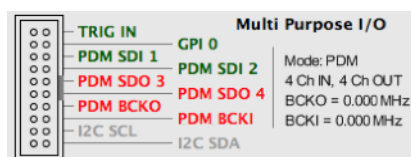


#### 1.4.1. Multi Purpose I/O

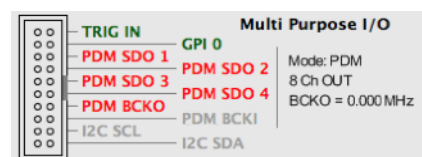
By default, the multi-purpose IOs are configured as input pins. Their state is captured on every frames. When the audio hardware interface option is available, the pins can be configured as serial data lines and clock lines.



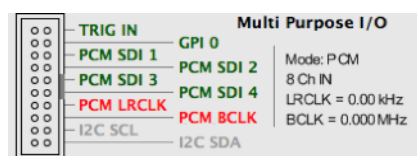
8 Channel PDM inputs



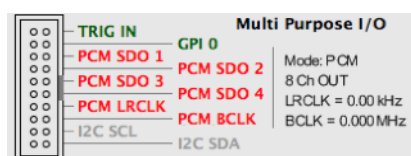
4 Ch PDM in and 4 Ch PDM out



8 Channel PDM outputs



8 Channel PCM inputs



8 Channel PCM outputs

The operation mode is indicated as well as the bit and word clocks (from release 1.27 and upwards).

## 1.4.2. SoundWire I/O

This part of the display shows the measured bus frequency, the status of the bus hold and the SoundWire signalling voltage. When activity is detected on a pin, the display shows a yellow circle in place of the corresponding pin (grey by default).

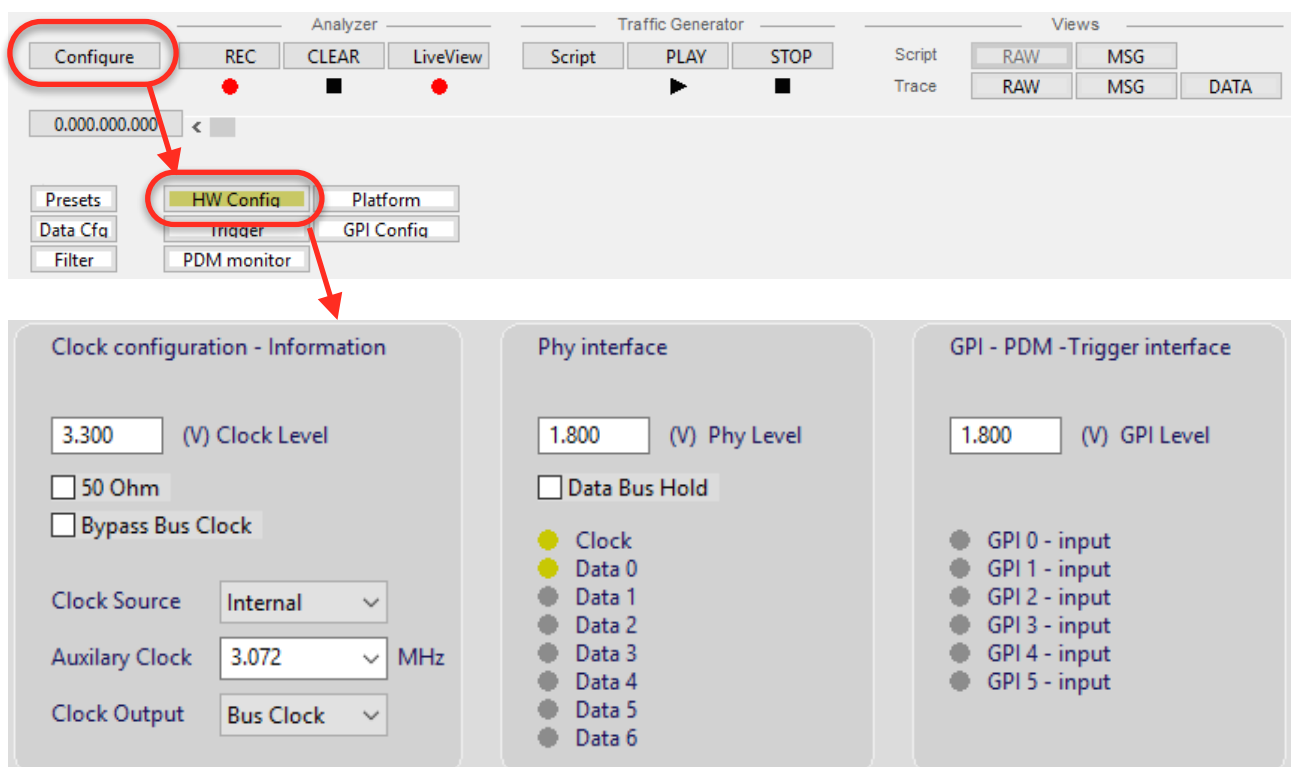
## 1.4.3. Clock I/O

The hardware can input a clock signal on a SMA RF connector and output a clock signal on another SMA RF connector.

The display shows the clock IO configuration and functions as well as the measured clocks.

## 1.5. Hardware Parameter Control

All of these parameters can be controlled by a script, when the tool is used as a traffic generator (see the ScriptBuilder user manual) or in real time by the hardware control panel of the analyser software.



## 2. SOFTWARE OPERATION

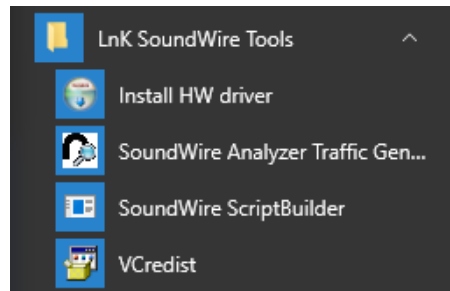
### 2.1. Installation

Double click on the installation software located on the USB memory stick.

It has a name in the form of LnK\_SoundWire\_Tools\_XXX.exe.

Note that it's always a good practice to copy the latest software release on the provided USB memory stick.

Once the installation is finished, go to the windows menu Program (in the task bar) and select LnK SoundWire Tools.



- Make sure the the HW unit is unplugged from any USB port of the PC.
- Run the Install HW driver application.
- In some cases, it might be required to install the Microsoft redistributable DLLs by running the VCredist application.
- Plug the USB license key (blue dongle) in any of the USB port of the host PC. Drivers installation is not required to operate the license dongle.
- Plug the hardware unit on a USB3 port (preferably) or a USB2 port.

The tools are ready for operation.

### 2.1. Software units

The tool uses 2 softwares:

- The SoundWire Protocol Analyzer & Traffic Generator. The present user manual is dedicated to this piece of software.
- The script editor (named ScriptBuilder) to generate XML scripts to be used by the Traffic Generator. ScriptBuilder also provide a very powerful capture post processing tool. Refer to the ScriptBuilder user manual for detailed explanation on the XML scripting tags.

### 2.2. Launching the Protocol Analyzer

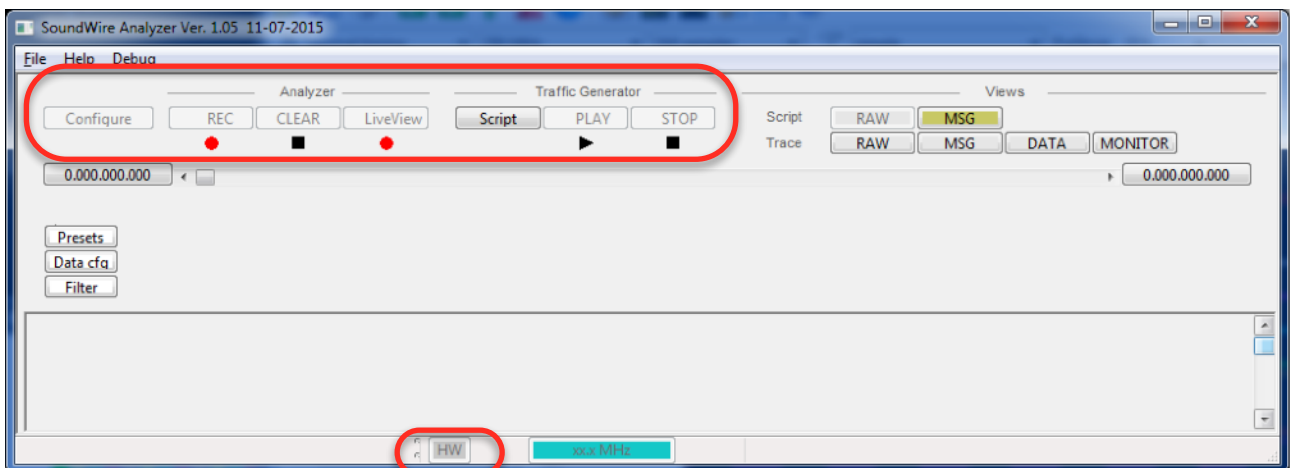
Make sure that the license key is plugged on a USB port of the host PC.

Launch the analyzer application.

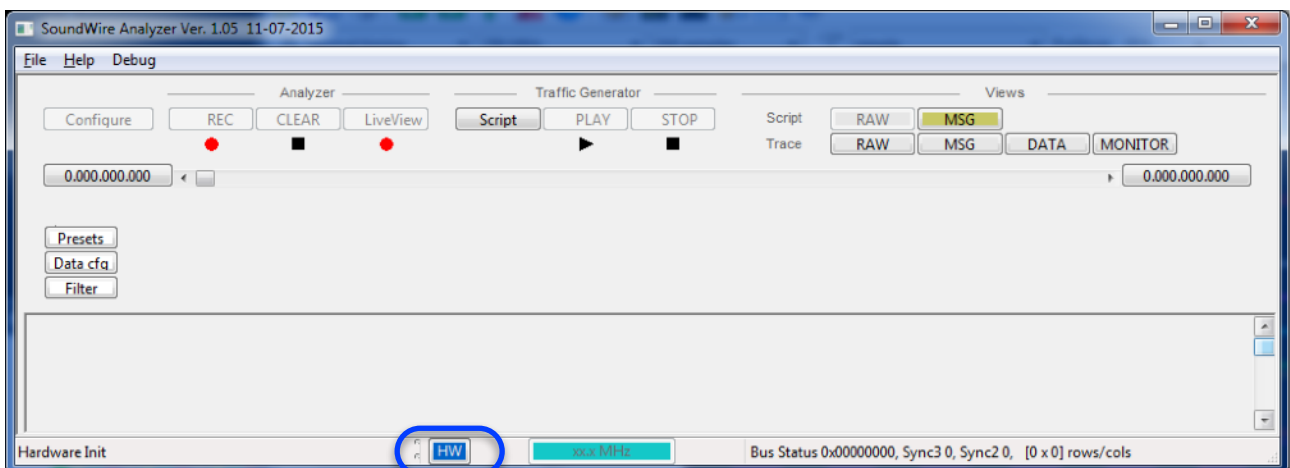
As soon as the application is running, it will search for the hardware unit and configure it.

As long as the hardware unit has not been detected and configured by the PC, its display will show a standby message asking for PC connection.

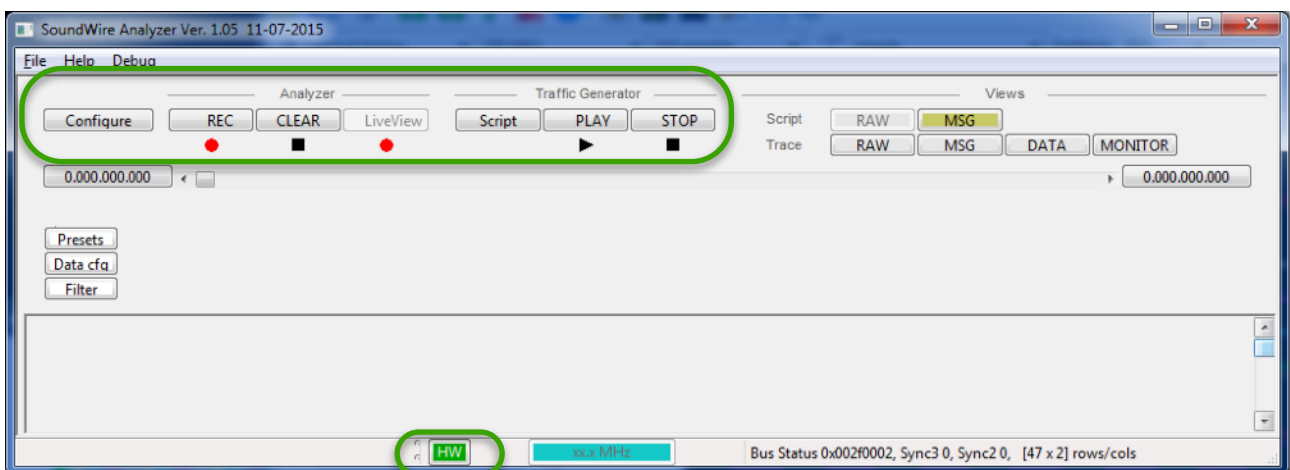
The HW status can be seen in the status bar at the bottom of the window. The hardware functions (like record and play) are greyed out if the hardware is not available.



**HW not present or non configured**



**HW detected and being configured**



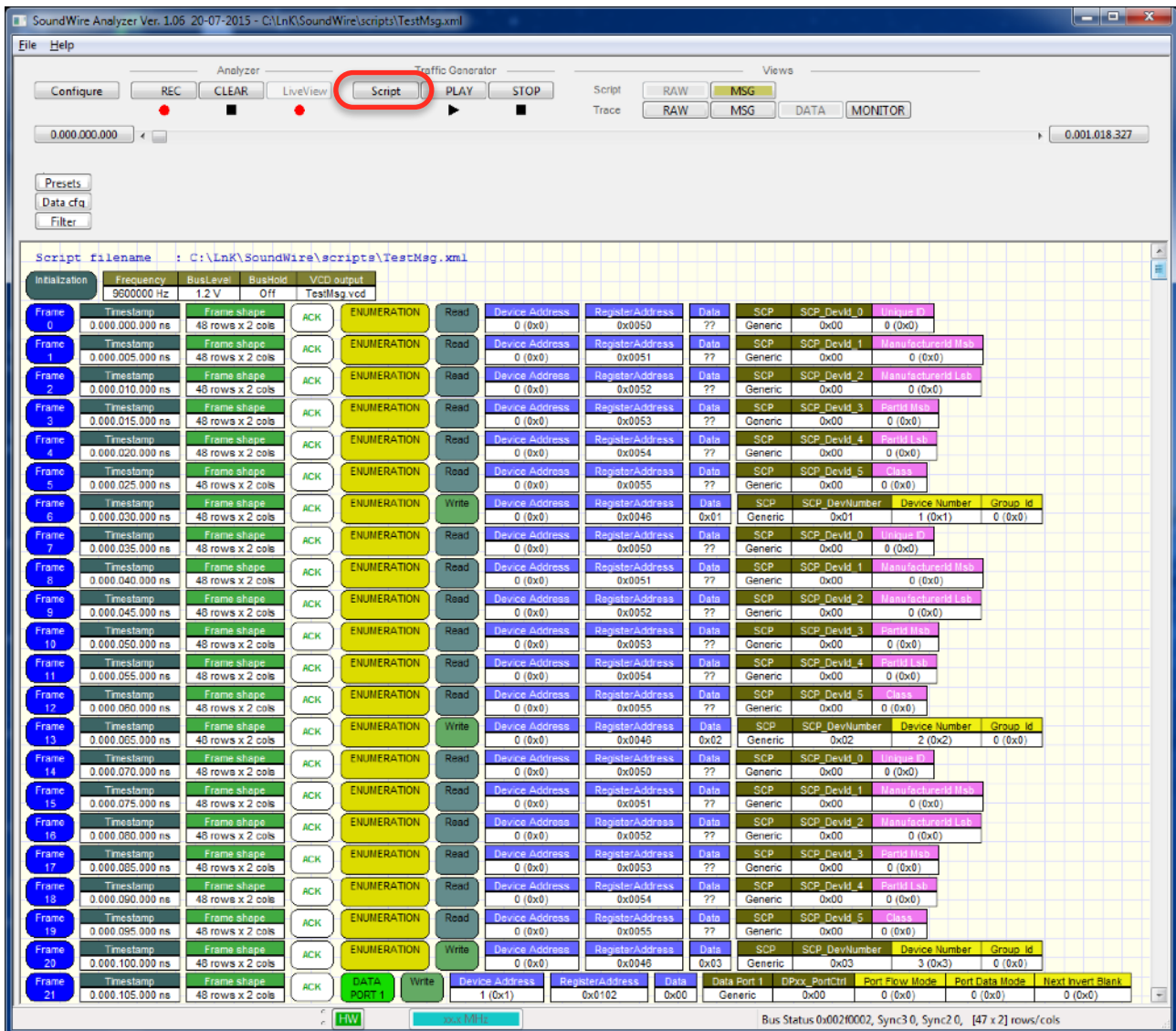
**HW detected and configured**



## 2.3. Load a script in the traffic generator

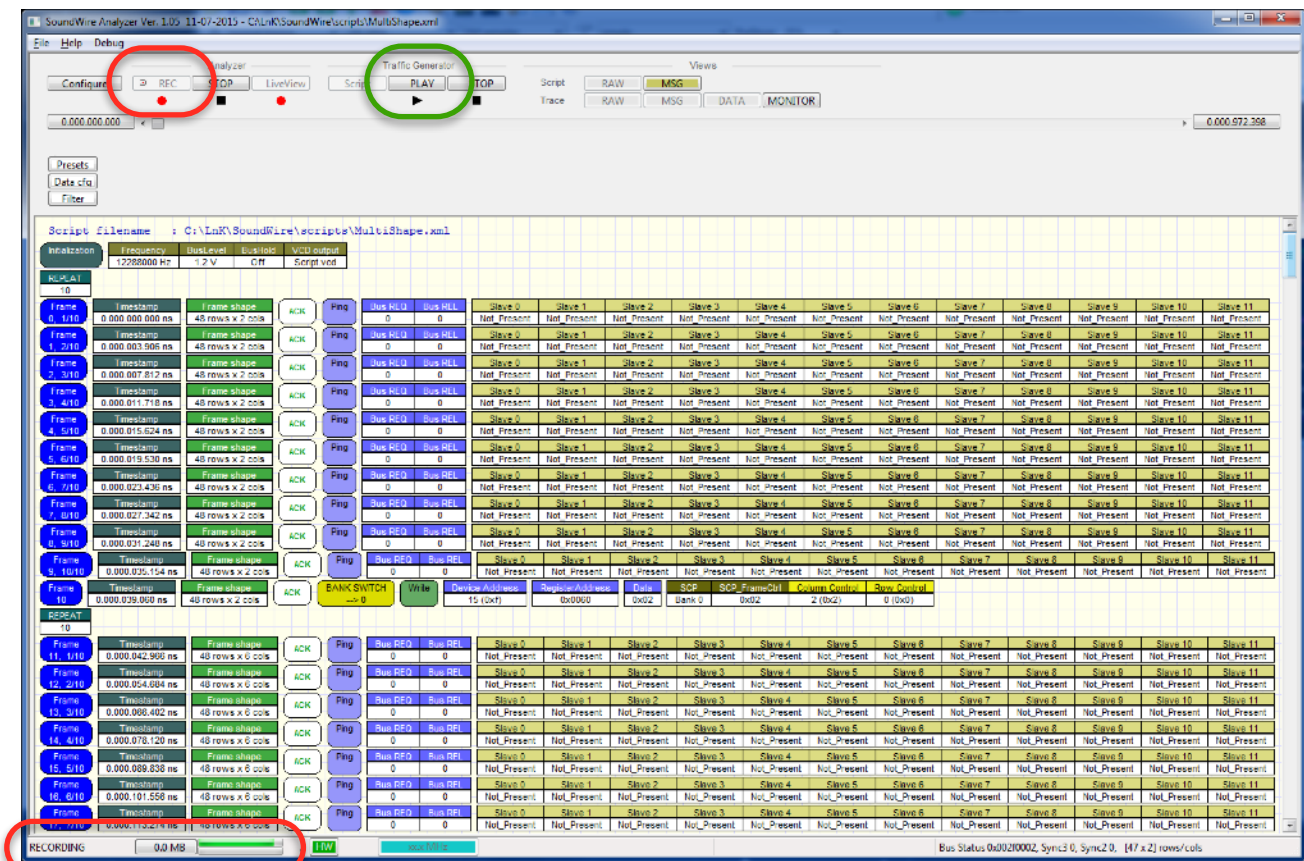
There are 2 ways to load a script in the traffic generator:

- Load an XML script from the traffic generator itself (through File menu or by pressing the Script button)
- Push it directly from the script editor (use CTRL+T or press the button **Send to TG** in the Finalize window).



The script content is shown in the main analyzer window.

## 2.4. Play and record a script

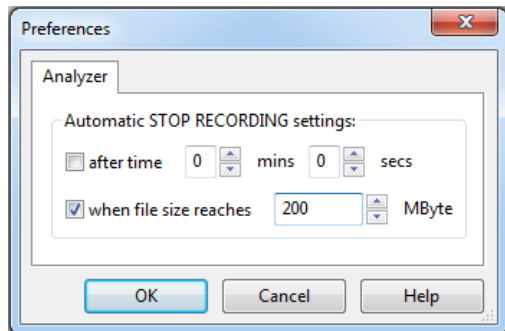


First press the **REC** button. Once pressed, it is greyed out. The analyzer is waiting for any clock activity on SoundWire to start the recording process. It's possible to stop the recording at any moment by pressing the **STOP** button besides the **REC** button. The amount of recorded data is shown in the status bar, on the bottom left side of the window. The maximum record size is now limited to 500 MB to prevent internal database files exceeding 4GB.

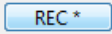
Then, press the **PLAY** button of the Traffic Generator to stream out the script. Once the script has been executed, press the **STOP** button of the analyzer to start the decoding of the recorded stream.

## 2.4.1. Recording options

File -> Preferences



Recording can be limited by defining a maximum time period or by a certain maximum file length. This is useful when recording is started due to a trigger event so only the relevant trace is being recorded and avoiding unnecessary long processing time and large files.

The REC button will have a '\*' added  when a limiting option is enabled.

## 2.4.2. Full recording mode

Full Recording is capturing all the bits from the bus and is able to reconstruct the complete trace and decoding and extracting all audio data.

This mode is consuming a lot of disk space and decoding time but gives the most detail.

While recording, the Live View is combined, so all relevant messages are shown on the screen while happening on the bus.

## 2.4.3. Live View

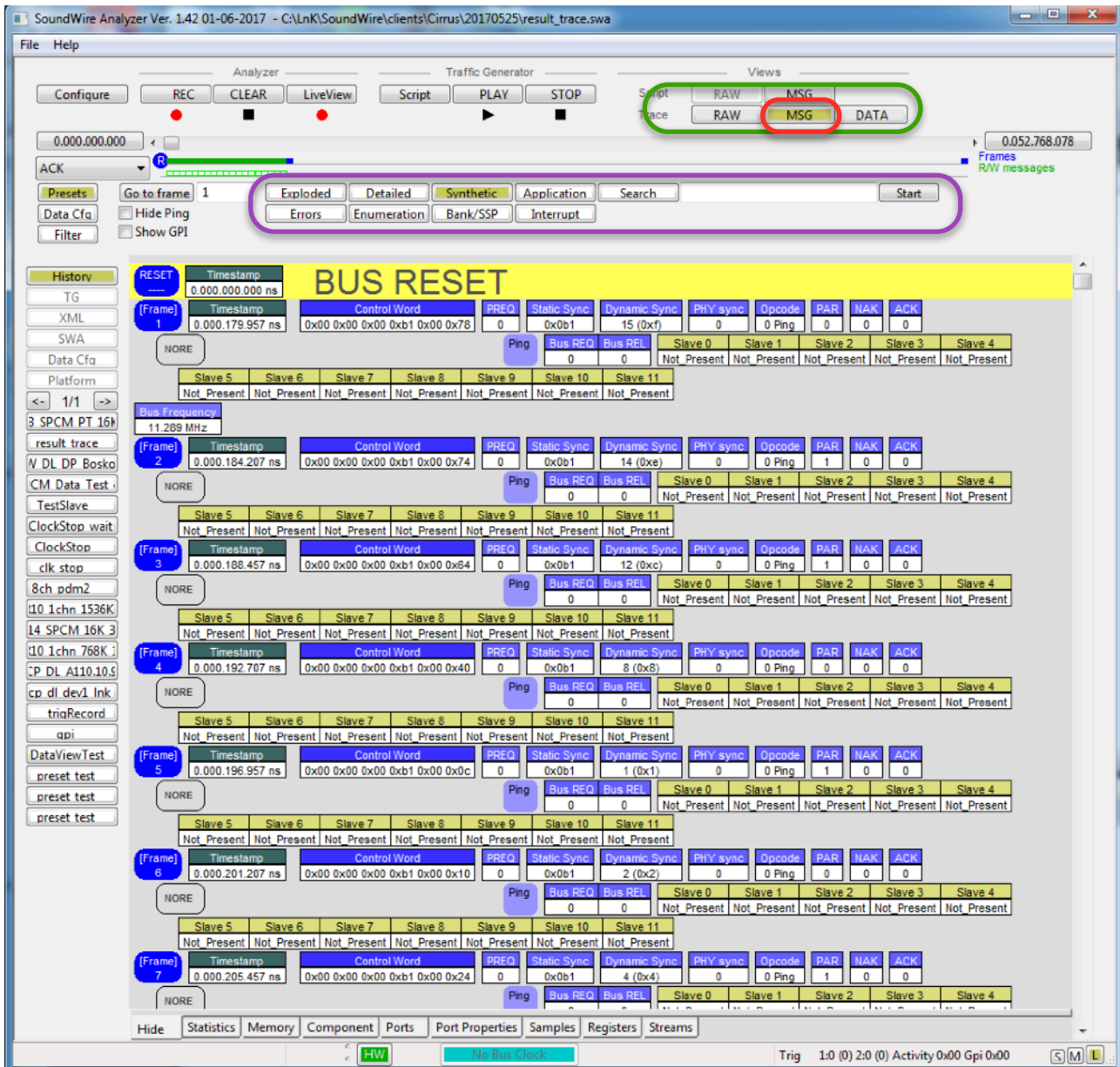
Live view is a monitor of all relevant messages captured from the bus. This mode is not capturing all the data bits from the bus thus it is not possible to reconstruct any audio data.

But the capturing of the messages is allowing to build up the configuration and show all detected data port and device configurations.

### 3. Stream analysis

The protocol analyzer software offers various levels of reading of the captured SoundWire bit stream.

#### 3.1.1. Message View



The Message View has multiple levels of analysis:

- **Exploded.** Each message is decoded at the bit level and displayed as such.

Frame	Timestamp	Control Word	PREQ	Static Sync	Dynamic Sync	PHY sync	Opcode	PAR	NAK	ACK
33	0.000.290.911 ns	0x3f 0x00 0x70 0xb1 0x03 0xe5	0	0x0b1	12 (0xc)	0	3 Write	1	0	1

ACK	BANK SWITCH → 1	Write	Device Address 15 (0xf)	RegisterAddress 0x0070	Data 0x07
-----	--------------------	-------	----------------------------	---------------------------	--------------

PREQ	Opcode	Device Address	Register Address	Static Sync	Phy sync	Data	Dynamic Sync	Parity	NAK	ACK
0	011	1111	0000000001110000	10110001	0	00000111	1100	1	0	1

- **Synthetic.** The messages are decoded and shown in a list.

[Frame]	Timestamp	Control Word	PREQ	Static Sync	Dynamic Sync	PHY sync	Opcode	PAR	NAK	ACK
3	0.000.173.307 ns	0x20 0x00 0x50 0xb1 0x00 0x61	0	0x0b1	12 (0xc)	0	2 Read	0	0	1

ACK	ENUMERATION	Read	Device Address 0 (0x0)	RegisterAddress 0x0050	Data 0x00	SCP	SCP_Devid_0	Unique ID 0 (0x0)
-----	-------------	------	---------------------------	---------------------------	--------------	-----	-------------	----------------------

[Frame]	Timestamp	Control Word	PREQ	Static Sync	Dynamic Sync	PHY sync	Opcode	PAR	NAK	ACK
4	0.000.177.216 ns	0x20 0x00 0x51 0xb1 0x00 0x41	0	0x0b1	8 (0x8)	0	2 Read	0	0	1

ACK	ENUMERATION	Read	Device Address 0 (0x0)	RegisterAddress 0x0051	Data 0x00	SCP	SCP_Devid_1	ManufacturerId Msb 0 (0x0)
-----	-------------	------	---------------------------	---------------------------	--------------	-----	-------------	-------------------------------

[Frame]	Timestamp	Control Word	PREQ	Static Sync	Dynamic Sync	PHY sync	Opcode	PAR	NAK	ACK
5	0.000.181.124 ns	0x20 0x00 0x52 0xb1 0x00 0x09	0	0x0b1	1 (0x1)	0	2 Read	0	0	1

ACK	ENUMERATION	Read	Device Address 0 (0x0)	RegisterAddress 0x0052	Data 0x00	SCP	SCP_Devid_2	ManufacturerId Lsb 0 (0x0)
-----	-------------	------	---------------------------	---------------------------	--------------	-----	-------------	-------------------------------

- **Application.** The frame information is hidden and messages only show the relevant information to understand the message flow.

[Frame]	Timestamp	ACK	ENUMERATION	Read	DA	SCP	SCP_Devid_0	Unique ID
3	0.000.173.307 ns	ACK	ENUMERATION	Read	0	Generic	0x00	0 (0x0)

[Frame]	Timestamp	ACK	ENUMERATION	Read	DA	SCP	SCP_Devid_1	ManufacturerId Msb
4	0.000.177.216 ns	ACK	ENUMERATION	Read	0	Generic	0x00	0 (0x0)

[Frame]	Timestamp	ACK	ENUMERATION	Read	DA	SCP	SCP_Devid_2	ManufacturerId Lsb
5	0.000.181.124 ns	ACK	ENUMERATION	Read	0	Generic	0x00	0 (0x0)

- **Errors.** All frames that are obtaining errors are listed here. That is easy to navigate to a certain error and then switch back to a more generic view such as Application view.

Frame	Timestamp	Static Sync	Dynamic Sync	NORE	Ping	Bus REQ	Bus REL	Slave 0	Slave 1	Slave 2	Slave 3	Slave 4	Slave 5	Slave 6	Slave 7	Slave 8	Slave 9	Slave 10	Slave 11
155453	0.627.150.232 ns					0	0	Not Present	Not Present	Not Present	Not Present	Not Present	Not Present	Not Present	Not Present	Not Present	Not Present	Alert	Not Present
155456	0.627.154.141 ns					0	0	Not Present	Not Present	Not Present	Not Present	Alert	Not Present	Not Present	Not Present	Not Present	Not Present	Not Present	Not Present

- **Enumeration.** Here all enumeration related events are shown.

RESET	Timestamp	BANK SWITCH	Slaves	Bank	SSP
---	0.000.000.000 ns	→ 1	0 1 2 3 4 5 6 7 8 9 10 11	1 1 1 1 1 1 1 1 1 1 1 1	12864 12864 12864 12864 12864 12864 12864 12864 12864 12864 12864 12864
Frame 135	0.000.750.374 ns	→ 1	0 1 2 3 4 5 6 7 8 9 10 11	1 1 1 1 1 1 1 1 1 1 1 1	5888 5888 5888 5888 5888 5888 5888 5888 5888 5888 5888 5888
Frame 159	0.001.015.403 ns	→ 0	0 1 2 3 4 5 6 7 8 9 10 11	0 0 0 0 0 0 0 0 0 0 0 0	256 256 256 256 256 256 256 256 256 256 256 256
Frame 161	0.001.038.091 ns	Ping SSP	0 1 2 3 4 5 6 7 8 9 10 11	0 0 0 0 0 0 0 0 0 0 0 0	256 256 256 256 256 256 256 256 256 256 256 256



- The diagram illustrates the timing of a bus reset sequence. It starts with a 'RESET' signal (yellow bar) and a 'Timestamp' column showing the time in nanoseconds. The sequence includes several 'ENUMERATION' frames (yellow bars) and a 'NORE' frame (grey bar). The 'ENUMERATION' frames are labeled 'Frame 21' through 'Frame 27'. The 'NORE' frame is labeled 'Frame 4'. The 'ENUMERATION' frames show a 'Timestamp' and an 'ACK' signal (green bar). The 'NORE' frame shows a 'Timestamp' and a 'NORE' signal (grey bar). The 'ENUMERATION' frames also show a 'Device Address' (0 (0x0)) and a 'RegisterAddress' (0x0050 through 0x0055). The 'NORE' frame shows a 'Device Address' (0 (0x0)) and a 'RegisterAddress' (0x0046). The 'ENUMERATION' frames also show a 'Data' field (0x01 through 0x02). The 'NORE' frame shows a 'Data' field (0x02). The 'ENUMERATION' frames also show a 'Slave 0' status (Attached\_OK) and a 'Slave 1' status (Not\_Present). The 'NORE' frame shows a 'Slave 0' status (Attached\_OK) and a 'Slave 1' status (Not\_Present). The 'ENUMERATION' frames also show a 'Slave 2' status (Not\_Present) and a 'Slave 3' status (Not\_Present). The 'NORE' frame shows a 'Slave 2' status (Not\_Present) and a 'Slave 3' status (Not\_Present).

RESET	Timestamp	BUS RESET			
---	0.000.000.000 ns				
[Frame] 4	0.017.011.871 ns	NORE			
Frame 21	0.023.390.721 ns	ACK	ENUMERATION		
Frame 22	0.023.765.719 ns	ACK	ENUMERATION		
Frame 23	0.024.140.728 ns	ACK	ENUMERATION		
Frame 24	0.024.515.727 ns	ACK	ENUMERATION		
Frame 25	0.024.890.725 ns	ACK	ENUMERATION		
Frame 26	0.025.265.724 ns	ACK	ENUMERATION		
Frame 27	0.025.640.733 ns	ACK	ENUMERATION		
Frame 28	0.026.015.731 ns	NORE			

Ping	Bus REQ	Bus REL	Slave 0	Slave 1	Slave 2	Slave 3
	0	0	Attached_OK	Not_Present	Not_Present	Not_Present

Read	Device Address	RegisterAddress	Data
	0 (0x0)	0x0050	0x01
Read	Device Address	RegisterAddress	Data
	0 (0x0)	0x0051	0x01
Read	Device Address	RegisterAddress	Data
	0 (0x0)	0x0052	0xc1
Read	Device Address	RegisterAddress	Data
	0 (0x0)	0x0053	0x12
Read	Device Address	RegisterAddress	Data
	0 (0x0)	0x0054	0x34
Read	Device Address	RegisterAddress	Data
	0 (0x0)	0x0055	0x00
Write	Device Address	RegisterAddress	Data
	0 (0x0)	0x0046	0x02

Ping	Bus REQ	Bus REL	Slave 0	Slave 1	Slave 2	Slave 3
	0	0	Attached_OK	Not_Present	Attached_OK	Not_Present

- The diagram illustrates the data flow and status for two frames (98 and 102) and two slave alerts (Slave 10 and Slave 4).

**Frame 98:** Timestamp: 0.052.265.847 ns. Data: DATA PORT 0. Write: DA. Read: DA. Data Port 0: DP0\_IntMask: 0xab, Test Fail: 1 (0x1), Port Ready: 1 (0x1), BRA failure: 0 (0x0), Imp-Def1: 1 (0x1), Imp-Def2: 0 (0x0), Imp-Def3: 1 (0x1).

**Frame 102:** Timestamp: 0.053.765.852 ns. Data: DATA PORT 0. Write: DA. Read: DA. Data Port 0: DP0\_IntMask: 0x00, Test Fail: 0 (0x0), Port Ready: 0 (0x0), BRA failure: 0 (0x0), Imp-Def1: 0 (0x0), Imp-Def2: 0 (0x0), Imp-Def3: 0 (0x0).

**Slave 10:** Alert: Slave 10. Status: Static Sync, Dynamic Sync, NORE, Ping.

**Slave 4:** Alert: Slave 4. Status: Static Sync, Dynamic Sync, NORE, Ping.

- Go to frame

1

Exploded

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da=1

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Interrupt

Show GPI

Frame 110	Timestamp	ACK	DATA PORT 1	Write	Device Address	RegisterAddress	Data	Data Port 1	DPxx_BlockCtrl1	Word Length
	0.000.644.085 ns				1 (0x1)	0x0103	0x1f	Generic	0x1f	31 (0x1f)
Frame 111	Timestamp	NORE	DATA PORT 1	Write	Device Address	RegisterAddress	Data	Data Port 1	DPxx_BlockCtrl2	Block Group Control
	0.000.648.350 ns				1 (0x1)	0x0131	0x00	Bank 1	0x00	0 (0x0)
Frame 112	Timestamp	ACK	DATA PORT 1	Write	Device Address	RegisterAddress	Data	Data Port 1	DPxx_SampleCtrl1	Sample Interval Low
	0.000.652.596 ns				1 (0x1)	0x0132	0xff	Bank 1	0xff	255 (0xff)
Frame 113	Timestamp	ACK	DATA PORT 1	Write	Device Address	RegisterAddress	Data	Data Port 1	DPxx_SampleCtrl2	Sample Interval High
	0.000.656.852 ns				1 (0x1)	0x0133	0x01	Bank 1	0x01	1 (0x1)
Frame 114	Timestamp	ACK	DATA PORT 1	Write	Device Address	RegisterAddress	Data	Data Port 1	DPxx_OffsetCtrl1	Offset1
	0.000.661.098 ns				1 (0x1)	0x0134	0x00	Bank 1	0x00	0 (0x0)
Frame 115	Timestamp	ACK	DATA PORT 1	Write	Device Address	RegisterAddress	Data	Data Port 1	DPxx_OffsetCtrl2	Offset2
	0.000.665.344 ns				1 (0x1)	0x0135	0x00	Bank 1	0x00	0 (0x0)

### 3.1.2. RAW View

The Raw View shows the frame shape and the content of every BitSlot. The BitSlots belonging to data stream are highlighted with different colors. The frame information and Control Word are shown for every frame. The unused bit slots are written in white. The configured bit slot from data channels are written in black with a color background representing their port. The first column contains the control word. If bit slots with a '1' value are detected in unconfigured data space they are coloured red to flag an error.

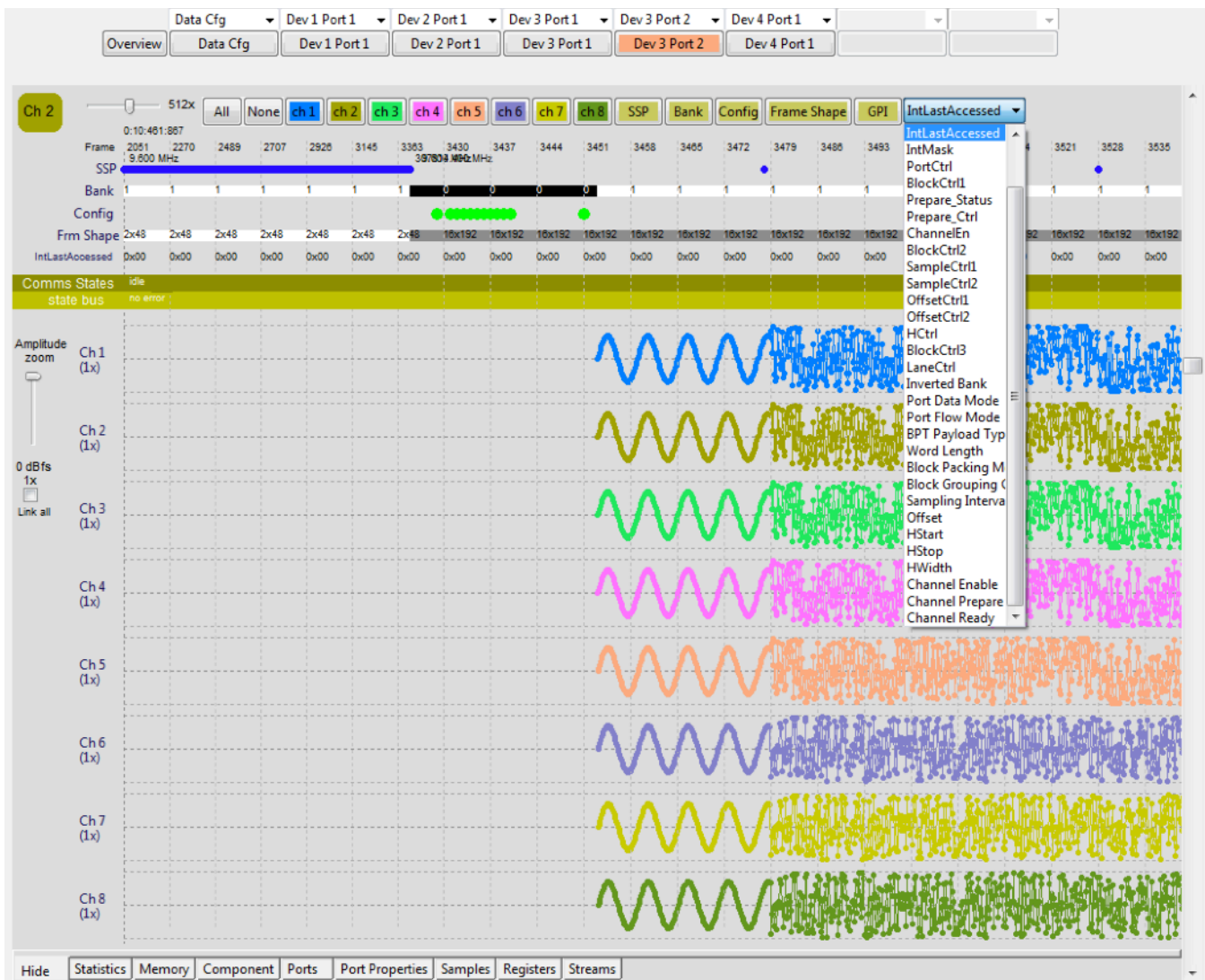
The screenshot displays the SoundWire Analyzer software interface. The 'RAW' view is selected in the 'Views' tab. The main display area shows a frame structure with the following columns: Control Word, PRE0, Static Sync, Dynamic Sync, PHY sync, Opcode, PAR, NAK, ACK, and 12 Slave ports (Slave 0 to Slave 11). The frame data is displayed in a grid format with bit values (0 or 1) and color-coded backgrounds (yellow for configured, red for unconfigured). The frame information at the top indicates a timestamp of 0.003180911 ns and a control word of 0x00 0x00 0x00 0xb1 0x02 0x0c. The frame data shows a sequence of bits for each port, with some ports (Slave 0 to Slave 11) showing 'Not Present' or 'Attached OK'.

Frame	Timestamp	col / row	Control Word	PRE0	Static Sync	Dynamic Sync	PHY sync	Opcode	PAR	NAK	ACK
350	0.003180911 ns	cols 4 rows 64	0x00 0x00 0x00 0xb1 0x02 0x0c	0	0x0b1	1 (0x1)	0	0 Ping	1	0	0

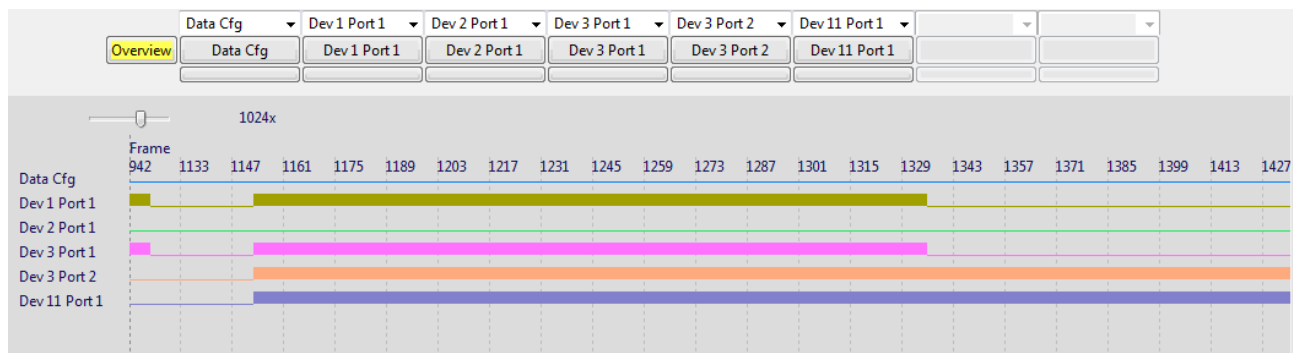
The frame data is displayed in a grid format with bit values (0 or 1) and color-coded backgrounds (yellow for configured, red for unconfigured). The frame data shows a sequence of bits for each port, with some ports (Slave 0 to Slave 11) showing 'Not Present' or 'Attached OK'.

### 3.1.3. DATA View

The main purpose of the DATA View is to show the configuration and content of the different data streams active on the SoundWire bus at a given moment in time.

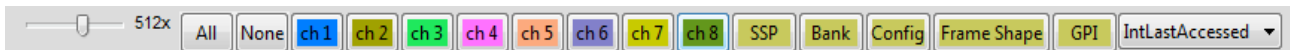


Up to 7 configured data ports are mapped onto the data port selection buttons together with a user “Data Config” button. If there are more than 7 configured data ports they are selectable through the listbox above every port button.





Display options:



- Time zoom factor: 1x - 32768x
- Channel selection: All, None, all available channels
- SSP: Stream Synchronisation Point indicated by a blue dot
- Bank: the current selected Bank alternating background of black and white with the value of the bank
- Config: A yellow dot show a write operation to the SCP or Data port registers
- Frame Shape: Shows the frame shape on an alternating background color. ex 2x48
- GPI: General Purpose Inputs are shows as defined in the GPI config. As 1 line or as a bus.
- A system or data port register values are displayed over the time line

### 3.1.4. Info notebook

There is a Info notebook at the bottom of the views. Default it is hidden.



## 1. Statistics

This page shows an overview of message and bus events as seen at the end of the recording.

Statistics

	Number		Write	Read	NAK	ACK	No Response
Lost Frames	7	Total	126	24	0	153	0
Frames	183378	Slave 0	4	24	0	28	0
Sync lost		Slave 1	26	0	0	26	0
Parity error		Slave 2	22	0	0	22	0
Ping	183228	Slave 3	47	0	0	47	0
Invalid Opcode		Slave 4	0	0	0	0	0
		Slave 5	0	0	0	0	0
		Slave 6	0	0	0	0	0
		Slave 7	0	0	0	0	0
		Slave 8	0	0	0	0	0
		Slave 9	0	0	0	0	0
		Slave 10	0	0	0	0	0
		Slave 11	23	0	0	23	0
		Group ID 12	0	0	0	0	0
		Group ID 13	0	0	0	0	0
		Monitor	0	0	0	0	0
		Broadcast	4	0	0	7	183223

Hide

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## 2. Memory Inspector

The memory inspector has two modes. The RAW mode which is showing the register values in Hex for the last read in green and last write operation in blue separately. The last action is drawn in bold. Note that this values are taken out of the read and write messages on he bus which is not a guarantee that the register is still containing the indicated values.

A general memory map shows the complete 64K range and also the different data port and system area are selectable together with eventual define regions of specific devices. See component editor of script builder,

RAW mode:


Memory inspector




RAW 0. Device 0 General map Address range [0x0000 - 0xFFFF]

Address	0x0 Rd Wr	0x1 Rd Wr	0x2 Rd Wr	0x3 Rd Wr	0x4 Rd Wr	0x5 Rd Wr	0x6 Rd Wr	0x7 Rd Wr	0x8 Rd Wr	0x9 Rd Wr	0xA Rd Wr	0xB Rd Wr	0xC Rd Wr	0xD Rd Wr	0xE Rd Wr	0xF Rd Wr
0x0000																
0x0010																
0x0020																
0x0030																
0x0040																
0x0050	0xA1	0xB2	0xC3	0xD4	0xE5	0xF6										
0x0060							0x0B									
0x0070																
0x0080																
0x0090																
0x00A0																
0x00B0																
0x00C0																
0x00D0																
0x00E0																
0x00F0																

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Decoded mode indicates the name of the register and has all the bit fields explained as written in the SoundWire specification so it is clear what was written to or read from that register.

Memory inspector 

Decoded 1. LnK AmpData port 1

Address range [0x0100 - 0x01FF]

Address	Name	Hex		bit 7		bit 6		bit 5		bit 4		bit 3		bit 2		bit 1		bit 0	
		Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr
0x0100	DPxx_IntStat/Clear Generic DP 1					Imp-Def3	Imp-Def2	Imp-Def1			-	-	-				Port Ready	Test Fail	
0x0101	DPxx_IntMask Generic DP 1					Imp-Def3	Imp-Def2	Imp-Def1			-	-	-				Port Ready	Test Fail	
0x0102	DPxx_PortCtrl Generic DP 1	0x00			0		0		0		0		0		0		0	0	0
0x0103	DPxx_BlockCtrl1 Generic DP 1	0x00			0		0		0		0		0		0		0	0	0
0x0104	DPxx_Prepare_Status Generic DP 1																		
0x0105	DPxx_Prepare_Ctrl Generic DP 1	0x00			0		0		0		0		0		0		0	0	0
0x0106	Reserved Generic DP 1																		
0x0107	Reserved Generic DP 1																		
0x0108	Reserved Generic DP 1																		
0x0109	Reserved Generic DP 1																		

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When A component has defined in the component library (via script builder or xml) then specific regions are added to the choice list.

Memory inspector

Decoded1. LnK Amp

Amp Registers set 1

Address range [0x0007 - 0x0014]

Address	Name	Hex		bit 7		bit 6		bit 5		bit 4		bit 3		bit 2		bit 1		bit 0	
		Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr	Rd	Wr
0x0007	Reserved Generic DP 0					-	-			-	-					-	-		
0x0008	Reserved Generic DP 0					-	-			-	-					-	-		
0x0009	Reserved Generic DP 0					-	-			-	-					-	-		
0x000a	Reserved Generic DP 0					-	-			-	-					-	-		
0x000b	Reserved Generic DP 0					-	-			-	-					-	-		
0x000c	Reserved Generic DP 0					-	-			-	-					-	-		
0x000d	Reserved Generic DP 0					-	-			-	-					-	-		
0x000e	Reserved Generic DP 0					-	-			-	-					-	-		
0x000f	Reserved Generic DP 0					-	-			-	-					-	-		
0x0010	Reserved Generic DP 0					-	-			-	-					-	-		

Amp Registers set 1

Amp Registers set 2

General map

Control - Data 0 port

Data port 1

Data port 2

Data port 3

Data port 4

Data port 5

Data port 6

Data port 7

Data port 8

Data port 9

Data port 10

Data port 11

Data port 12

Data port 13

Data port 14

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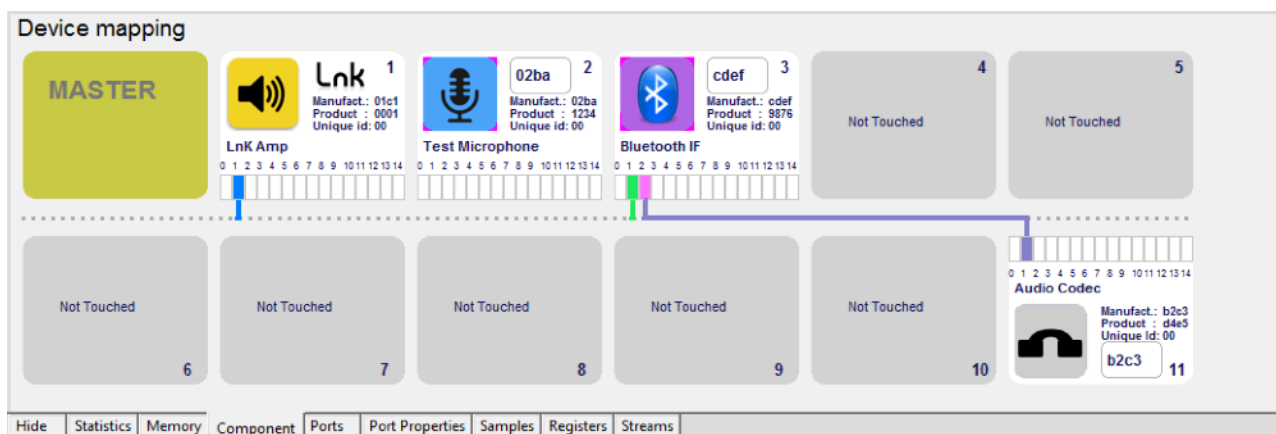
Registers

Streams

### 3. Device Mapping

The software can detect the different devices on the bus and displays them with the enumeration information and data port use. Enabled data ports are indicated and if data ports have the same configuration, they will be connected together. This option is very handy during the live view and so a device map with data port activity will be up to date on what is happening on the bus.

If a full recording has been done or a \*.swa or an \*.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor.



## 4. Ports Mapping

In this page are all the detected data ports. If the data port is not enabled it is displayed with a thin circle and when it is enabled, it is indicated by a thick circle. If data ports have the same configuration they are drawn as connected. If a full recording has been done or a \*.swa or an \*.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor. When the analyser is in live view, the page is showing the current situation of the bus.



## 5. Port Properties

In this page the data port configuration parameters are shown. The active bank is high lighted. If a full recording has been done or a \*.swa or \*.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor. When the analyser is in live view, the page is showing the current situation of the bus.

Port properties

11. Device 11 Port 1

	Common	Bank 0	Bank 1	Comment
Used Bank	1			Indicated Bank (1) * Inverted Bank (0) = Used Bank (1)
Port Data Mode	0			Normal operation
Port Flow Mode	0			Isochronous
BPT Payload Type				Only available on data port 0
Word Length	24 bit(s)			
Block Packing Mode		0	0	Block per Port
Block Grouping Control		1	1	Used BlockGroupCount = 1
Sampling Interval		1 (0x0001)	512 (0x0200)	
Offset		0x0000	0x0000	Offset = 0 (0x0000)
HStart		0	3	
HStop		15	10	
Sample Rate	-	-	-	Info not available
Channel Enable			87654321	Chan 8 -> Chan 1
Channel Prepare	87654321			Chan 8 -> Chan 1
Channel Ready				Chan 8 -> Chan 1
Lane		0	0	

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## 6. Data Samples

This page is only valid when loading a \*.swa or \*.fvf file or when done a full recording.

Data samples											
11. Device 11				Port 1							
Frame	Bit Offset	Sample Length	Flow Control	Chan 1	Chan 2	Chan 3	Chan 4	Chan 5	Chan 6	Chan 7	Chan 8
122189	42	24		0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
122189	554	24		0x000bd3f0	0x00177414	0x000bd3f1	0x002d4efa	0x0010b514	0x00085253	0x00019b8b	0x004e7a06
122189	1088	24		0x00177412	0x002d4efb	0x00177413	0x004e7a05	0x002120fa	0x00101379	0x0000c8d1	0x004e7a07
122189	1578	24		0x0022ad79	0x0040136f	0x0022ad79	0x005a9df7	0x0030fbc5	0x0016bc27	0x00003718	0x00000000
122189	2090	24		0x002d4efb	0x004e7a07	0x002d4efa	0x004e7a06	0x003ffffe	0x001bd835	0x0002c8d1	0x00b185fa
122189	2602	24		0x00372a06	0x00578783	0x00372a05	0x002d4efb	0x004debe4	0x001f0e7b	0x00019b8b	0x00b185fa
122170	42	24		0x0040136f	0x005a9df7	0x00401370	0x00000000	0x005a8279	0x000202f3	0x00000000	0x00000000
122170	554	24		0x0047e42e	0x00578782	0x0047e42e	0x00d2b106	0x00858c9a	0x001f0e7b	0x00f8e474	0x004e7a06
122170	1088	24		0x004e7a06	0x004e7a06	0x004e7a07	0x00b185f9	0x008e99ea	0x001bd836	0x00f8372e	0x004e7a07
122170	1578	24		0x0053b81f	0x0040136f	0x0053b820	0x00a56209	0x007841af	0x0016bc28	0x00f8e474	0x00000000
122170	2090	24		0x00578783	0x002d4efc	0x00578783	0x00b185f9	0x007ba373	0x00101379	0x00f8372d	0x00b185f9
122170	2602	24		0x0059d780	0x00177412	0x0059d780	0x00d2b105	0x007ee7a9	0x00085253	0x00f8e475	0x00b185f9
122171	42	24		0x005a9df6	0x00000000	0x005a9df5	0x00000000	0x007ffffe	0x00000000	0x00000000	0x00000000
122171	554	24		0x0059d780	0x00e88bec	0x0059d780	0x002d4efb	0x007ee7a9	0x00f7adac	0x00019b8c	0x004e7a05
122171	1088	24		0x00578782	0x00d2b105	0x00578783	0x004e7a07	0x007ba373	0x00efec96	0x0002c8d1	0x004e7a06
122171	1578	24		0x0053b81f	0x00fec91	0x0053b81f	0x005a9df7	0x007841af	0x00e943d8	0x00003718	0x00000000
122171	2090	24		0x004e7a07	0x00b185fa	0x004e7a06	0x004e7a06	0x008e99ea	0x00e427ca	0x0002c8d1	0x00b185f9
122171	2602	24		0x0047e42e	0x00a8787d	0x0047e42d	0x002d4efb	0x00858c98	0x00e0f184	0x00019b8b	0x00b185f9
Hide				Statistics	Memory	Component	Ports	Port Properties	Samples	Registers	Streams

## 7. Port Registers

In this page the data port registers are shown in decimal, hexadecimal and binary. The active bank is high lighted.

If a full recording has been done or a \*.swa or \*.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor. When the analyzer is in live view, the page is showing the current situation of the bus.

Port registers				
11. Device 11		Port 1		
	Common	Bank 0	Bank 1	Comment
IntStat	0 - 0x00 - 0b00000000			
IntClear	0 - 0x00 - 0b00000000			
IntLastAccessed	0 - 0x00 - 0b00000000			
IntMask	0 - 0x00 - 0b00000000			
PortCtrl	0 - 0x00 - 0b00000000			
BlockCtrl1	23 - 0x17 - 0b00010111			
Prepare Status	0 - 0x00 - 0b00000000			
Prepare Ctrl	255 - 0xff - 0b11111111			
ChannelEn	0 - 0x00 - 0b00000000	255 - 0xff - 0b11111111		
BlockCtrl2	0 - 0x00 - 0b00000000	0 - 0x00 - 0b00000000		
SampleCtrl1	0 - 0x00 - 0b00000000	255 - 0xff - 0b11111111		
SampleCtrl2	0 - 0x00 - 0b00000000	1 - 0x01 - 0b00000001		
OffsetCtrl1	0 - 0x00 - 0b00000000	0 - 0x00 - 0b00000000		
OffsetCtrl2	0 - 0x00 - 0b00000000	0 - 0x00 - 0b00000000		
HCtrl	15 - 0x0f - 0b00001111	58 - 0x3a - 0b00111010		
BlockCtrl3	0 - 0x00 - 0b00000000	0 - 0x00 - 0b00000000		
LaneCtrl	0 - 0x00 - 0b00000000	0 - 0x00 - 0b00000000		
Hide		Statistics	Memory	Component
		Ports	Port Properties	Samples
		Registers	Streams	

## 8. Stream Mapping

The Stream Mapping table shows all the data ports for all the slave devices. If a data port is used, it is coloured. When it is active, it wil contain a stream number. All the data ports that have the same number are connected.

If a full recording has been done or a \*.swa or \*.fvf has been loaded, the content is dynamically updated according to the position of the time line cursor. When the analyzer is in live view, the page is showing the current situation of the bus.

Stream mapping															
	Device	DP 0	DP 1	DP 2	DP 3	DP 4	DP 5	DP 6	DP 7	DP 8	DP 9	DP 10	DP 11	DP 12	DP 13
1	LnK Amp		0												
2	Test Microphone														
3	Bluetooth IF		2	3											
4															
5															
6															
7															
8															
9															
10															
11			3												
Hide		Statistics	Memory	Component	Ports	Port Properties	Samples	Registers	Streams						